POWER ANALYSIS OF 6T SRAM CELL AT DEEP SUB-MICRON TECHNOLOGY

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ABSTRACT

With continuous advancements in technologies, the SRAM memories have undergone changes with respect to decrease in geometric cell size, increased transistor density and high frequency. Such circuits consume an excessive amount of power. In this paper the power analysis of a conventional 6T SRAM cell is carried out in 90 nm process technology. The power dissipation of the SRAM cell during read, write operations and in standby mode are observed and then transistor stacking is applied to the inverters in the SRAM cell. The simulations are done at various supply voltages from 0.7 v to 1.0 v. Simulation results show much reduction in standby power dissipation after the application of stacking technique to the SRAM circuit. The circuits have been simulated using HSPICE with BSIM4 MOSFET models.

Key words: Standby mode, stacking effect, power dissipation, process technology, 6T SRAM cell

I. INTRODUCTION

As we move deeper in the sub-micron region, scaling of both the supply voltage and threshold voltage of transistors will cause a significant increase in the sub-threshold static leakage current due to its exponential relationship to the threshold voltage. This results in increased leakage power dissipation, which was almost 44% of the total power consumed in the Intel 's' Pentium III processor. The power consumed in high performance microprocessors has increased to levels that impose a fundamental limitation to increasing performance and functionality (1) & (2). SRAM is an important part of modern microprocessor design, taking a large portion of the total chip area and power. Increasing the density of SRAM caches provides an effective method to enhance system performance. According to the ITRS-2003, 90% of the chip area will be occupied by the memory core by 2014 (3). This shows the demand for chips with low power SRAMS. In SRAMS the static power consumption is due to leakage currents. Therefore it is important to focus on minimizing the leakage power in SRAM structures. There have been many efforts both at the architectural and circuit level to deal with the leakage problem in SRAM circuits. In this work the power dissipation of a six transistor SRAM cell during standby mode, read operation and write operation are analyzed. The proposed SRAM cell uses transistor stacking in the inverters to reduce the standby and active power during read and write operations in the memory. The rest of the paper is organized as follows: In section II related work in the area of SRAM power minimization is presented. Section III gives the basic operation of SRAM cell and section IV presents the proposed SRAM cell. In section V the simulation results are discussed and section VI gives the conclusion.

II. RELATED WORK IN SRAM CELL

Researchers in the static memory design domain have reported several integrated circuit and architecture level approaches to address the power and performance in deep-sub-micron CMOS technologies. In (4) G. Razavipour, et al. proposed the PP SRAM Bit – Cell structure where the two nMOS access transistors have been replaced by the two High-Vt pMOS access transistors. It utilizes the dual threshold voltage technology with Forward Body Biasing (FBB) to reduce the sub-threshold leakage without loosing the performance. In (5) B. Amelifard, et al. proposed an architecture of the SRAM Bit-cell by inserting an extra nMOS transistor in between the ground line and SRAM cell, called as the Gated- Ground technique to reduce the leakage power consumption in the high performance cache memories with single Vt (transistor threshold voltage) process. In (6) K. Nil et al. proposed Multiple Threshold CMOS Technique (MT-CMOS) to influence the leakage current. In the active mode of the operation of the memory cell, the low threshold voltage is preferred because of the higher performance. However, in the standby mode of operation, high threshold voltage is useful for reduction of the leakage power. In (7) N. Azizi et al. has proposed an asymmetric SRAM cell design in 70nm technology. In this an nMOS transistor is added to the SRAM bit-cell

to reduce the magnitude of the gate voltage when the cell stores data '0'. In comparison with the conventional SRAM bit-cell, the gate leakage of the proposed structure decreases in the '0' state while it increases in the '1' state. P. Elakkumanan et al. in (8) has suggested the NC-SRAM design at 65 nm technology. It employs Dynamic Voltage Scaling (DVS) Scheme to reduce the leakage power of the SRAM bit-cells while retaining the stored data during the idle mode. Kyeong-Sik Min et al. described a row-by-row dynamic source line voltage control (RRDSV) scheme in (9). A negative word line method for leakage reduction is presented by Chua-Chin Wang et al. in (10) and K. Fujita et al. proposed a floating body cell with open bit lines in deep sub-micron regime in (11).

III. A 6T SRAM CELL OPERATION

The schematic diagram of 6T SRAM cell is shown in Fig 1. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters formed by transistors P1, N1 and P2, N2. This storage cell has two stable states that are used to denote 0 and 1. Two additional access transistors A1 and A2 serve to control the access to storage cell during read and write operations. Access to the cell is enabled by the word line (WL) which controls the two access transistors, which in turn, control whether the cell should be connected to the bit lines: BL and BLB. They are used to transfer data for both read and write operations. While it's not strictly necessary to have two bit lines, both the signal and its inverse are typically provided since it improves noise margins. The operation of a SRAM cell is defined in three modes: Standby (hold) mode, read mode and write mode.

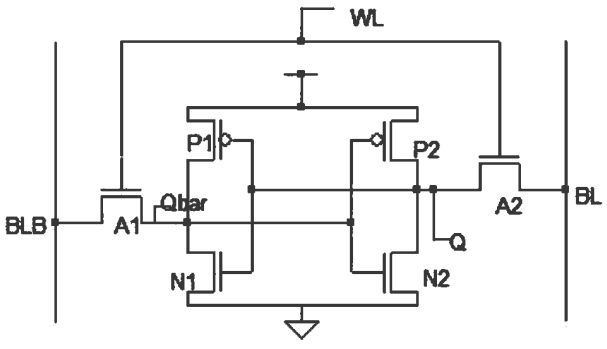

Fig. 1. Schematic diagram of a 6T SRAM cell

A. Standby mode

In this mode WL = 0. The two access transistors A1 and A2 disconnect the cell from bit lines BL and BLB. The two cross-coupled inverters formed by N1, P1 and N2, P2 will continue to reinforce each other as long as they are disconnected from the outside world. The current drawn in this state from the power supply is termed as standby current.

B. Write Mode

The two bit lines BL and BLB are used for writing data into the SRAM cell. To write data '1', BL is asserted high and BLB is asserted low and then word line WL is asserted high. Similarly for a write '0' operation BL = 0, BLB = 1 and WL is asserted high.

C. Read mode

Initially the bit lines BL and BLB are pre-charged to Vdd and then WL is asserted high. This turns on the access transistors A1 and A2 and the values of Q and Q bar are transferred to the bit lines BL and BLB respectively. A sense amplifier is used to sense the logic levels in a SRAM.

IV. PROPOSED WORK

In this work transistor stacking effect is used for decreasing the leakage power which is the main source of static power in SRAM memory cells. The leakage current flowing through a stack of series connected transistors reduces when more than one transistor of the stack is turned OFF. This effect is known as the "Stacking Effect" (12). If natural stacking of transistors do not exist in a circuit, then to utilize the stacking effect a single transistor of width W is replaced by two transistors each of width W/2. In the 6T SRAM cell, the transistors P1 and N1 form inverter1 and transistors P2 and N2 form the inverter2.The stacking technique is applied to these two inverters. Each NMOS transistor of width Wn is replaced by two NMOS transistors of width Wn/2 and each PMOS transistor of width Wp is replaced with two PMOS transistors of width equal to Wp/2. This produces self-reverse bias effect that in turn increases the threshold voltage Vt of the transistors. This increase in Vt decreases the leakage through the transistor and hence the reduction in standby mode current and power. Figure 2 shows the 6T SRAM cell with stacked transistors in the inverters.

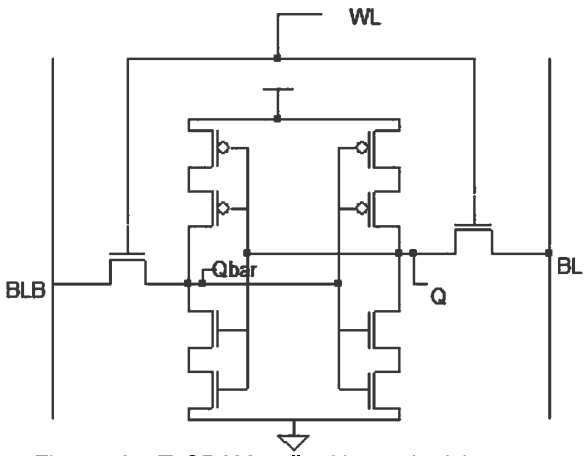

Fig. 2. A 6T SRAM cell with stacked inverters

V. SIMULATION RESULTS

In this paper, the power dissipated by a 6T SRAM cell during read operation, write '0' and write '1' operation and stand by mode are analyzed for two cases: Base case (conventional 6T SRAM cell) and with transistor stacking. The netlists of the circuits are extracted and simulated with BSIM4 models of MOSFETs. The simulations are done in HSPICE at a temperature of 27 degree centigrade. The supply voltage Vdd is varied from 0.7 v to 1.0 v. The read, write and stanby power are tabulated in Table 1 for the base case and in Table 2 for a SRAM cell with transistor stacking technique. The simulation results shows that the write '0' and write '1' power decreases

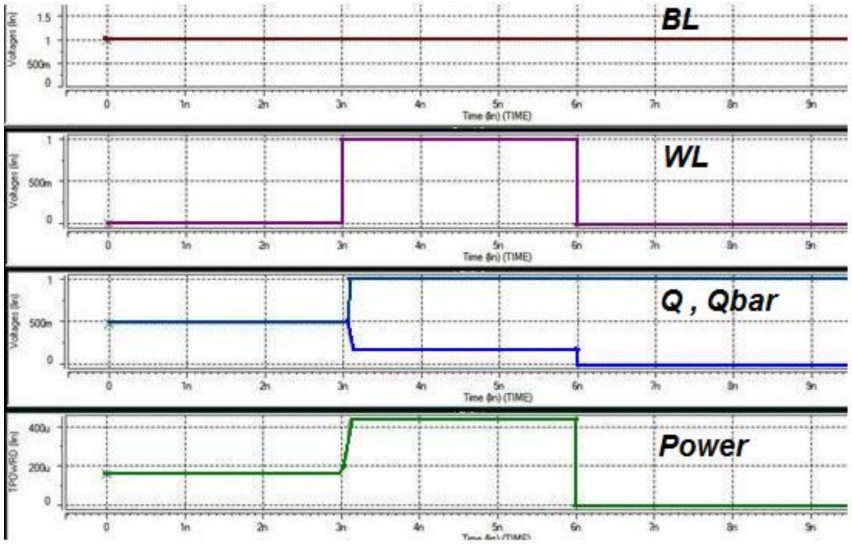

Fig. 3. Waveforms of SRAM read operation

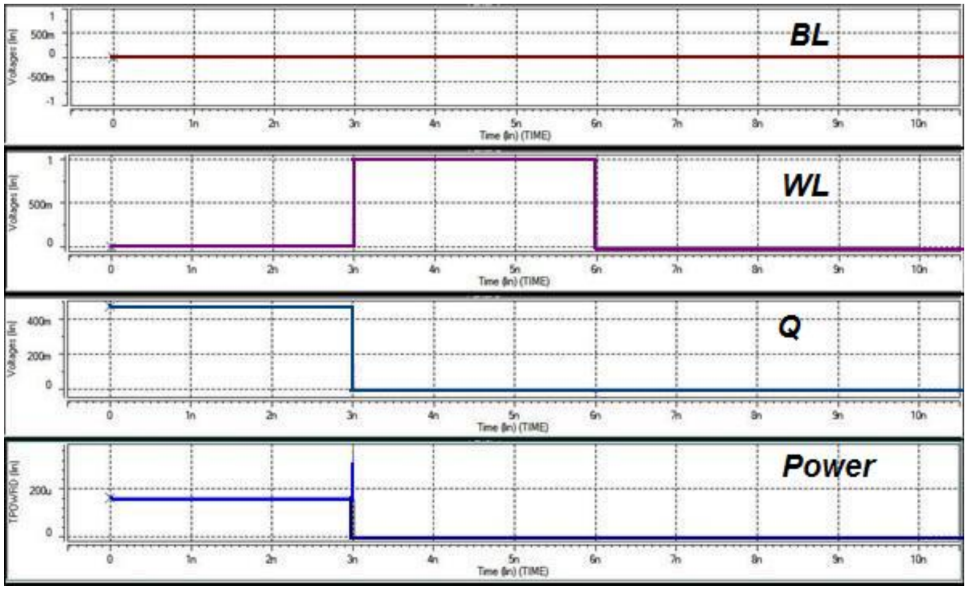

Fig. 4. Waveforms of SRAM write '0'

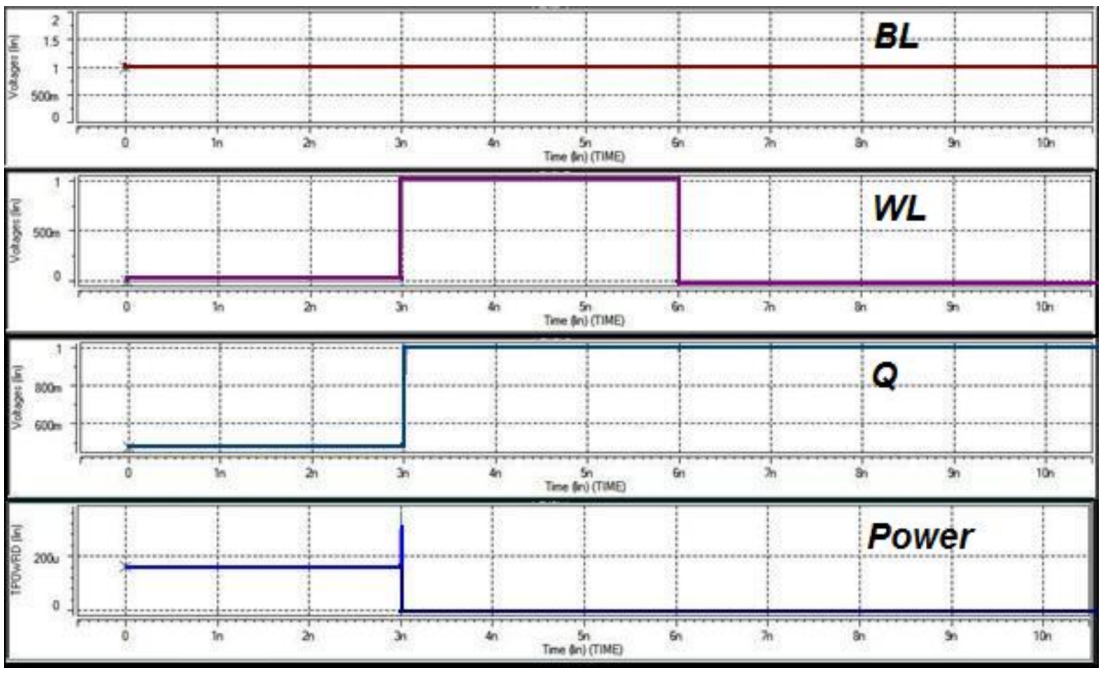

Fig. 5. Waveforms of SRAM write '1'

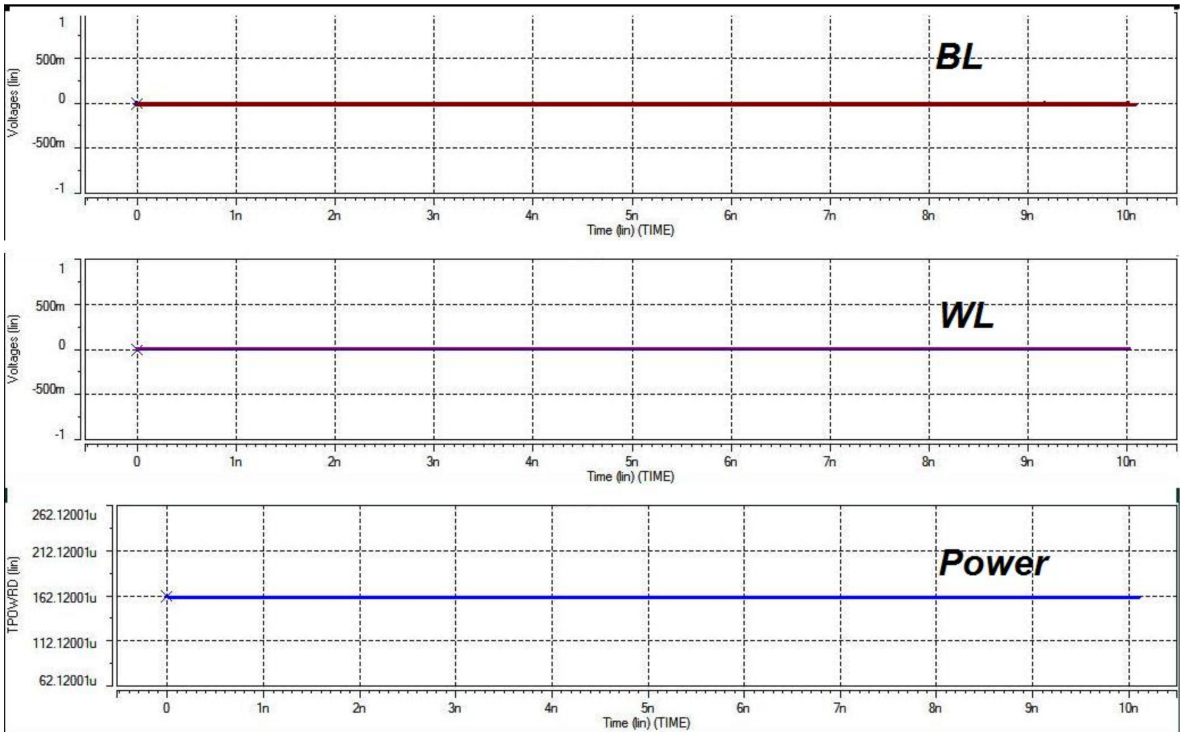

Fig. 6. Waveforms of SRAM In standby mode

by nearly 80% both at Vdd = 0.7 v and 1.0 v. In the case of read operation at Vdd = 1 v the decrease is 81.2% and at 0.7 v, the reduction is only 60.62%. In standby mode the power reduces from 1.62E-04 W to 6.25 nW at 1 V and from 1.45E-05 to 1.24 nW when Vdd = 0.7 V. Thus in all the three modes of operation with stacking effect the power reduces in the voltage range from 0.7 v to 1.0 v. Figures 3, 4 and 5 shows the waveform of SRAM cell during read, write '0' and write '1' operations respectively and Fig. 6 shows

standby mode waveforms. Fig. 7 & Fig. 8 shows the standby power of SRAM cell without & with the transistor stacking technique.

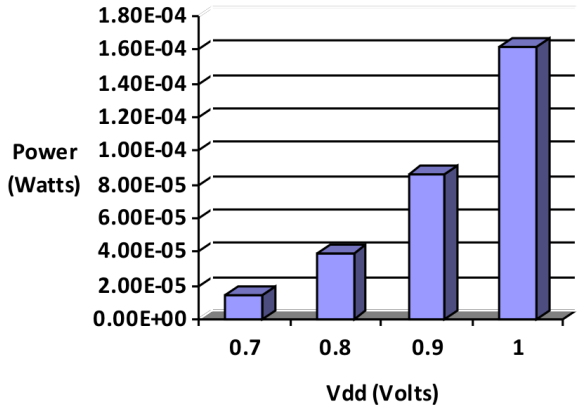

Fig. 7. SRAM standby power

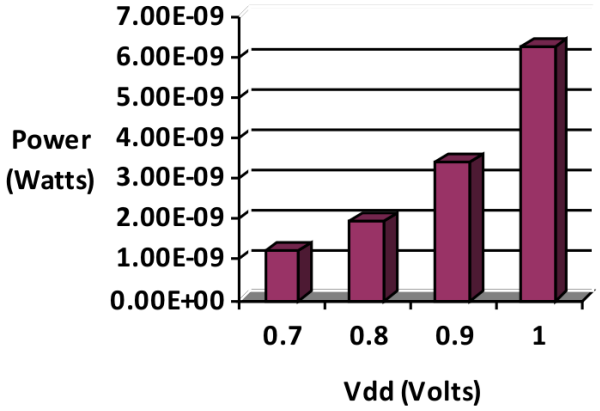

Fig. 8. Standby power with transistors stacking

Table 1
Power dissipation of SRAM cell

Operation	Power dissipation at different Vdd in watts			
	Vdd = 0.7 v	0.8 v	0.9 v	1.0 v
Write '0'	1.04E-04	1.64E-04	2.59E-04	3.62E-04
Write '1'	1.01E-04	1.62E-04	2.57E-04	3.48E-04
Read mode	1.29E-04	2.12E-04	3.15E-04	4.36E-04
Standby mode	1.45E-05	3.91E-05	8.65E-05	1.62E-04

Table 2
Power dissipation of SRAM cell with transistor stacking

Operation	Power dissipation at different Vdd in watts			
	Vdd = 0.7 v	0.8 v	0.9 v	1.0 v
Write '0'	1.62E-06	2.21E-06	2.83E-06	3.38E-06
Write '1'	1.60E-06	2.24E-06	2.68E-06	3.52E-06
Read mode	5.08E-05	6.12E-05	7.54E-05	8.19E-05
Standby mode	1.24E-09	1.97E-09	3.43E-09	6.25E-09

VI. CONCLUSION

Power reduction of a conventional SRAM cell with transistor stacking is proposed in this work. The read, write and standby mode power dissipation of SRAM cell with and without transistor stacking is analyzed in 90 nm process technology with BSIM 4 models of MOSFET. The simulations are done by varying the supply voltage from 0.7 v to 1.0 v. The results show much reduction in stand by mode power. The read and write power also decreases with the proposed technique.

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