DESIGN AND SIMULATION OF 2.4 GHZ CMOS LC VOLTAGE CONTROLLED OSCILLATOR WITH HIGH OUTPUT VOLTAGE SWING

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ABSTRACT

This paper presents the design and analysis of a 2.4 GHz Voltage Controlled Oscillator (VCO), with high output voltage swing for wireless communication applications. The oscillation frequency and the start-up conditions are derived. Accurate simulation of the VCO is performed in the software environments and the results are provided. A good agreement is seen between the simulation results and the derivation. This VCO operates at 2.4 GHz, achieves a peak to peak voltage of 0.758 volts with a low power consumption of 0.461 mA from a power supply voltage of 0.6 volts. The simulated VCO produces frequency tuning from 1.82GHz to 2.60 GHz (32.5%) with a control voltage varying from 0-0.3 volts. The output power level of the VCO is -8 dBm, with an improved predicted quality factor of 60.

Keywords: Variable capacitor, high output voltage swing, low power consumption, ultra low supply voltage

I. INTRODUCTION

Low power, low voltage integrated circuits have received stringent requirements in the area of modern communication circuits such as wireless transceivers, filters, low noise amplifiers and high frequency oscillators. With the demand of high band width and high speed communication channels, wireless transceivers, especially those working in GHz frequencies, call for VCOs with outstanding performance [1-2]. The performance properties of the VCOs are phase noise, frequency tuning range, power consumption, tuning sensitivity, spectral purity, load pulling, supply pulling, output power, harmonic suppression, output oscillation amplitude, and chip size. With the advancements in micromachining techniques the chip size can be reduced to several micro meters [3]. The tuning range of the VCO depends on the tuning elements like capacitors and inductors. By integrating these elements on single chip together with CMOS components, the tuning range may be improved [4-6]. The performance measure of an oscillator is its quality factor, i.e. the ratio of the resonant frequency peak to its spectral bandwidth. This performance indicator can be improved by decreasing the phase noise, since quality factor and the phase noise are inversely proportional to each other. Several works had been demonstrated to improve the major performance factors such as power consumption [7-8], and phase noise [9-10]. The objective of this paper is to develop a VCO which operates with considerable improvement in all these factors.

II. BACKGROUND

Parallel-plate MEMS variable capacitors along with a discrete commercially available 8.2 nH inductor and a separately-fabricated CMOS circuit were attached to a test board surface and wire-bonded to form the VCO [11]. This prototype oscillated at a center frequency of 714 MHz and could be tuned from 707 to 721 MHz over a DC voltage of 5.5 V. The phase noise was -107 dBc/Hz at an offset frequency of 100 kHz. Another VCO prototype with the same MEMS variable capacitors and a 5 mm-long bond wire 6 nH inductor were tested. It achieved -105 dBc/Hz phase noise at 100 kHz offset frequency from a 1.028-GHz carrier. The oscillator could be tuned over 20 MHz with 3 V and consumed 3.8 mA from a 3.3 V supply [12]. A 1.9-GHz CMOS VCO prototype, where the resonant circuit consisted of micromachined electromechanically tunable capacitors and a 3.5 nH bond wire, was implemented in a MUMPs polysilicon surface micromachining process. The active circuits were fabricated using a $0.5-\mu m$ CMOS process. The VCO was assembled in a ceramic package where the MUMPs and CMOS chips were connected using wire bonds. The experimental VCO achieved a phase noise of -98 dBc/Hz and -126 dBc/Hz at 100 kHz and 600 kHz offsets from the carrier, respectively. The tuning range of the VCO was 9%. The VCO circuit and the output buffer consumed 15 and 30 mW from a 2.7-V power supply, respectively [13-15].

III. PROPOSED VCO TOPOLOGY

The LC VCO is designed to oscillate at 2.4 GHz, and to determine the impact on the performance parameters. Fig. 1 shows the proposed VCO circuit. The cross coupled differential topology is utilized for the design to achieve large output voltage swing. From the well known theory of oscillators, the positive feedback transistors M_3 and M_4 are used to achieve negative input resistance, with which positive resistance of LC resonant circuit might be eliminated bringing on zero-dampen oscillating property. PMOS transistors M_1 and M_2 are used to generate the required bias current. MOS transistors M_6 and M_7 provide DC offset to the differential pairs. The output of the VCO is passed through a band pass filter to reduce the out-of-band noise level of the output signal. A resonant circuit with high quality factor, Q, is necessary to obtain low phase noise and is realized using Micro/Nano Electro Mechanical elements. The MOS transistors (M_1-M_7), the fixed capacitors (C_1-C_2), and the buffer circuit are realized using CMOS technology. An output buffer circuit, Ibuf, is designed to deliver maximum power to 50 ohms load.

A. Modified VCO design considerations

LCVCO provides outstanding phase noise and jitter performance at high frequencies compared to other topologies. Cross coupled pair LCVCO topology is selected for this design due to its high output voltage swing, balanced differential output and symmetrical structure. However this topology provides the above merits, it contains an inductor and a varactor in its tank circuit which are large area components. In order to reduce the die area of the resonant circuit, MWCNT based pulse inductor is integrated with Micro scale varactor. In order to reduce the required supply voltage and to eliminate additional noise contribution, the tail current transistors in a conventional cross-coupled VCO can be replaced by on-chip inductors as reported in [16]. In this work the tail current transistors are replaced with MWCNT bundle based inductor. For an enhanced voltage swing under an ultra-low supply voltage, the capacitive-feedback technique can be employed [17]. The capacitive feedback loop is established by C_1 and C_2. Due to the use of the on-chip inductor and the capacitive feedback loop, the drain and source voltages can swing above the supply voltage and below the ground potential. Consequently, the output swing of the VCO is enhanced, leading to a superior close-in phase noise. Since the feedback capacitors are employed in the source terminals of the cross-coupled transistors, a more effective controlled mechanism of the tank resonance is presented. Therefore, a reasonable frequency tuning range can be achieved even with a reduced voltage range for the controlled signal. Fig. 2 shows the schematic and the circuit of the

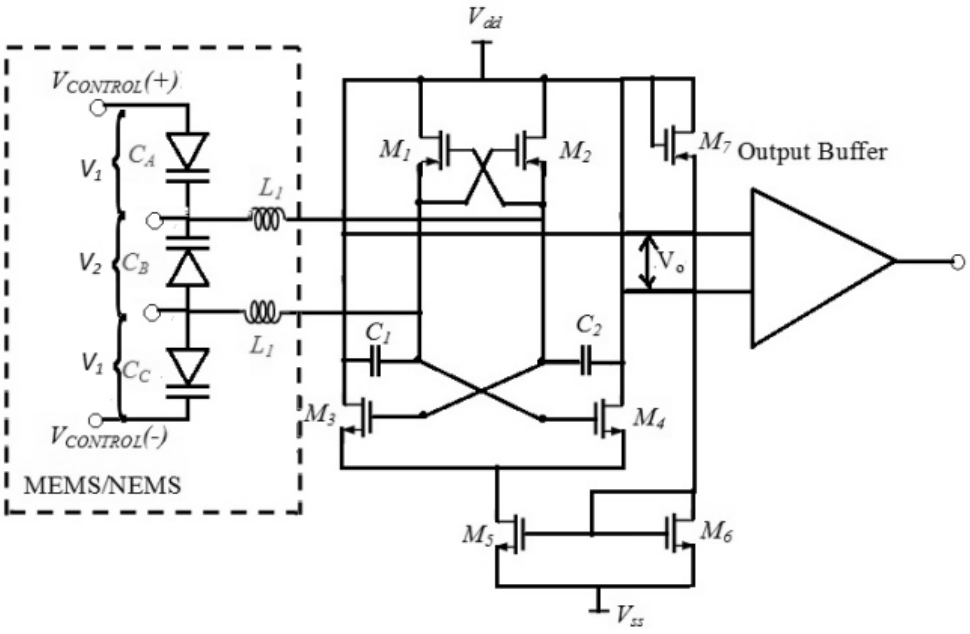

Fig. 1. Proposed differential VCO topology with micro machined tank circuit

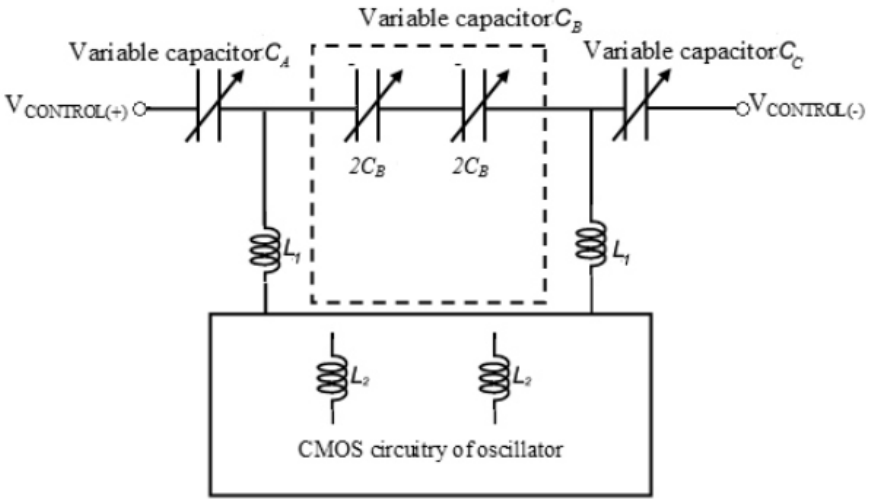

Fig. 2: (a) Schematic of the NEMS/MEMS Oscillator showing the symmetry of the design

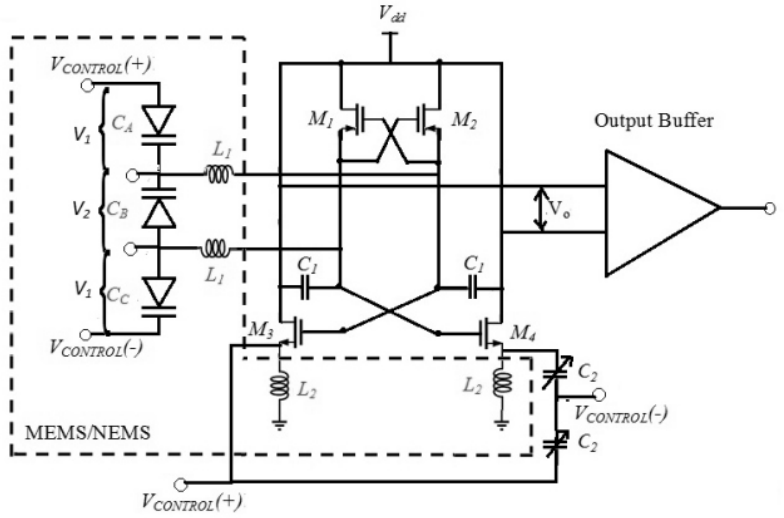

Fig. 2: (b) NEMS/MEMS oscillator circuit without tail current transistors

MEMS/NEMS oscillator. The variable capacitors C_A, C_B and C_C represent the Micro scale varactor and C_B is modelled as two series capacitances,to maintain the symmetry of the circuit. L_1 and L_2 are modelled as on-chip inductors. To further investigate the proposed VCO, detailed circuit analysis is provided in the fore coming sessions.

Considering the cross-coupled feedback oscillator as a one-port representation, the negative resistance seen at the drain of M3 and M4 can be computed as,

$$R_N = \frac{2}{g_m} \quad \text{... (1)}$$

It can inferred, that $|R_N|$ should be less than or equal to the equivalent parallel resistance of the tank in order to achieve sustained oscillations. Each individual MOS transistor in the differential pair is essentially a common source amplifier with a complex, tuned load comprised of a lossy inductor in parallel with a capacitor. As stated earlier the microscale capacitor [22] and the MWCNT based inductor[24] can be used to form the tank circuit otherwise the complex tuned load.

Fig. 3 illustrates the principle of LCVCO topology. The total impedance $Z_T$of the tank circuit is equal to $2Z_p$ since two tanks appear in series. The oscillation condition requires the closed loop gain should be at least unity magnitude and zero phase angle in addition to the cancellation of the positive conductance of the tank by the negative conductance of the active circuit.

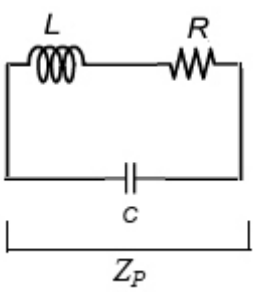

Fig. 3(a)

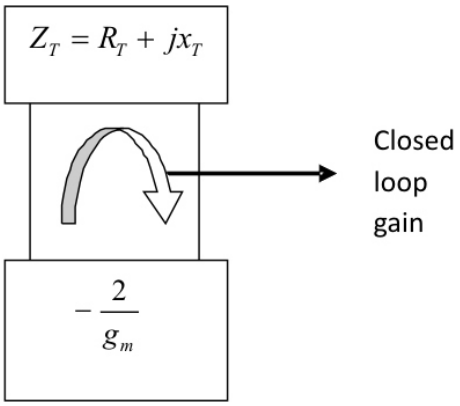

Fig. 3(b)

Fig. 3: Illustration of the LCVCO principle (a) Tank circuit equivalence with inductor loss modelled as series resistance (b) LCVCO principle of oscillation showing negative and positive impedance

Parallel resistance of the tank has to be cancelled out is given by,

$$R_T = Q\,2\,\pi\,fl_T \qquad \text{... (2)}$$

where $L_T$is the inductance of the tank, f is the frequency and $Q$is the resonator quality factor which could be improved using MEMS technology. The only loss assumed in equation (2) is due to the on-chip inductor, since inductors with low quality factor dominates the losses of the VCO tank. In reality there would also be losses associate with the variable capacitor and the MOSFETs. The resonator quality factor is given by,

$$Q_{\text{loaded}} = \frac{(t)_0}{(t)_1\,(t)_2} = \frac{R_T}{(t)_0\,l_T} \qquad \text{... (3)}$$

The loaded Q shown in equation (3) can be related with the component Q (Q_L and Q_C) as,

$$\frac{1}{Q_{\text{loaded}}} = \frac{1}{Q_1} + \frac{1}{Q_0} \qquad \text{... (4)}$$

The dimensions of the MOS transistors of active part have been calculated as,

$$\frac{W}{L} = \frac{g_m^2}{2\,KI_n} \qquad \text{... (5)}$$

The transconductance of the MOS transistor is given by the equation,

$$g_m = \frac{I_D}{V_{gs} - V_T} = 2k\frac{2}{L}L_D \qquad \text{... (6)}$$

From equations (3) and (4) it can be seen that the Q_{loaded} is approximately equal to the quality factor of the inductor Q_L, because often capacitors have much higher Q factor than inductors in integrated resonators. Equation (2) states that the effective resistive loss of the resonator R_T should be increased to increase the quality factor. The presence of losses results in a finite voltage swing over a narrow spread of frequencies. Also If R_T increases that further increases the size of the MOS transistor as in equation (5). Hence the suitable way of increasing the quality factor is by increasing Q_L.

B. Start-up conditions and oscillation frequency

The oscillation condition requires that the closed loop gain be at least unity magnitude and zero phase angle. The zero closed loop phase condition implied that at the frequency of oscillation, ω_0, $X_1(\omega_o) = 0$. The magnitude of the amplifier negative resistance must be at least as large as, $R_1(\omega_o) = 0$, the total resistive loss of the two tanks. Therefore by setting $X_1(\omega_o) = 0$, the value of ω_o can be determined and by setting $\left|\frac{1}{R_1(\omega_o)}\right| = \left|\frac{g_m}{2}\right|$, the minimum trans-conductance of each MOS transistor for oscillations to occur can be determined. In general the negative resistance of the differential pair MOS transistors must overcome all real resistive losses in the oscillator circuit. In order to derive the start-up conditions and the oscillation frequency, the equivalent

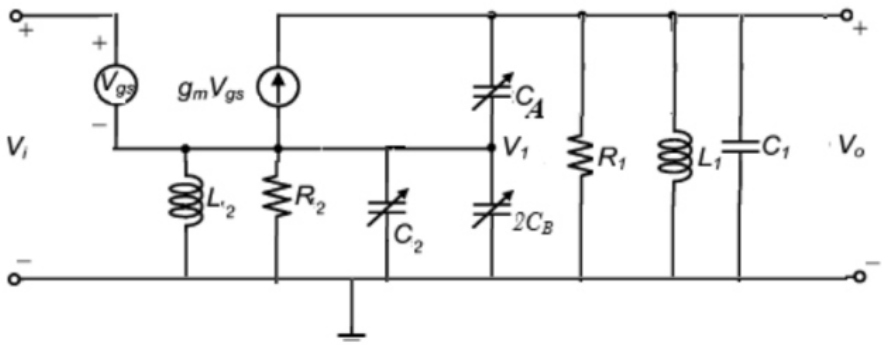

Fig. 4. Simplified half circuit model of the proposed VCO

half-circuit of the proposed VCO is shown in Fig. 4, where R_1 and R_2 represent the losses of the on-chip inductors L_1 and L_2, respectively. Note that the losses of the inductors are typically modelled by a series resistance (Fig. 3(a)).

In the equivalent circuit, the narrowband approximation is employed to simplify the analysis, and the shunt resistance R_1 and R_2 can be estimated by,

$$R_1 = \frac{\omega^2 l_3^2}{R_{s1}} \quad \text{... (7)}$$

$$R_2 = \frac{\omega^2 l_0^2}{R_{s2}} \quad \text{... (8)}$$

Using laplace transform analysis the approximated transfer function (single ended output to input) can be derived as,

$$\frac{V_0(S)}{V_1(S)} = \frac{g_m\left(b_0 S^2 + b_1 S^1 + b_3\right)}{a_0 S^4 + a_1 s^3 + a_2 S^2 + a_3 S + a_4} \quad \text{... (9)}$$

where the coefficients of the numerator and denominator are as follows:

$$C_e = C_2 // 2C_B$$

$$b_o = l_1 l_2 R_1 R_2 C_e$$

$$b_1 = l_1 l_2 R_1$$

$$b_2 = l_1 R_1 R_2$$

$$a_o = l_1 l_2 R_1 C_2 C_A C_e \quad \text{... (10)}$$

$$a_1 = l_1 l_2 C_1\left(R_1 C_A + R_2 C_A + R_2 C_e\right)$$

$$a_2 = R_1 R_2 C_1\left(l_3 C_A + l_3 C_A + l_2 C_e\right)$$

$$a_3 = C_1\left(l_1 R_2 + l_0 R_1 + g_m l_2 R_1 R_2\right)$$

$$a_4 = C_1 R_1 R_2 \quad \text{... (11)}$$

The circuit oscillates if equation (9)is equal to -1, and at the oscillation frequency ω_2,

$$g_m\left(b_0 \omega_o^2 + j b_1 \omega_o b_2\right) = a_0 \omega_o^4 - j a_1 \omega_o^3 - a_2 \omega_o^3 + j a_3 \omega_o + a_4 \quad \text{... (12)}$$

With proper assumptions and simplifications the oscillation frequency can be approximated as

$$\omega_o = \sqrt{\frac{1}{l_0 C_A} + \frac{2C_1\left(C_A + C_e\right)}{l_0 C_A C_B}} \quad \text{... (13)}$$

$$g_m = \frac{a_1 \omega_o^2 - C_1(l_1 R_2 + R_1 l_2)}{R_1 R_2\left(l_o - l_o\right) + b_o \omega_o} \quad \text{... (14)}$$

Assuming $L_1 = L_2 = L_P$ and $R_1 = R_2 = R_P$ equation (13) and (14) can be simplified as,

$$\omega_o = \sqrt{\frac{1}{l_p}\left[\frac{l}{C_A} + \frac{2C_1(C_A + C_e)}{C_A C_e}\right]}$$

$$g_m = \frac{l}{R_p}\left[1 + \frac{4(C_A/C_e)^3}{C_1 + l_p(C_A/C_e)}\right] \quad \text{... (15)}$$

From equation (13) it is seen that the oscillation frequency has two parts, in its theoretical derivation. As conventional LC Voltage Controlled Oscillators,

$\sqrt{\frac{1}{l_0 C_A}}$ contributes the major part of the oscillation frequency and the second part $\sqrt{\frac{2C_1 (C_A + C_e)}{C_A C_e}}$ further enhances the oscillation frequency. However, the fixed capacitance C_1 degrades the oscillation frequency compared to [18],could be still improved by the numerator part. From equation (15) it is noticed that the fixed capacitance C_1 increases (since < 1) the trans-conductance which helps us to initiate successful oscillations. Therefore, a design trade off is established between the tuning range and the trans-conductance based on C_1. Moreover, should be maintained to a value with which oscillations can occur. However a reasonable tuning range can be obtained using the four plate Micro scale varactor. It can be concluded that by selecting suitable and optimal values for the capacitors better theoretical performance can be seen from the designed oscillator.

C. Phase Noise

The devices that constitute the oscillator itself including active and passive components inject noise into an oscillator. The amplitude and the oscillation frequency will be affected by the noise injection. The amplitude noise will be stabilized by the non-linearities of the circuit. On the other hand, a random deviation in the frequency can also be viewed as a random variation in the zero crossing points of the time-dependant waveform. The output of the oscillator can be modeled mathematically as,

$$\gamma(t) = A \cos\left[\omega_o l + \phi_o(t) \right] \quad \text{... (16)}$$

Where $\gamma(t)$ is the output signal of oscillator, $\gamma(t)$ A is the noiseless oscillator amplitude, is the oscillator frequency, ϕ_n and is the phase noise. Phase noise is defined to quantify the fluctuations in frequency domain, and expressed as the ratio of the single side-band power at a frequency offset ω from the carrier with a measurement bandwidth of 1Hz to the carrier power. The formula of phase noise can be expressed as ,

$$L\Delta\omega = 10 \log\left[\frac{2FKT}{P_{\text{carrier}}} \frac{2\omega}{(Q_1 \Delta\omega)^2} \right] \quad \text{... (17)}$$

where K is the Boltzmann's constant, T the absolute temperature,Fan empirical parameter, P carrier the output power of carrier, Q_t the quality factor of the tank, ω_o the oscillation frequency, and $\Delta\omega$ is the offset frequency from the oscillation frequency [19]. According to equation (17), a high-Q tank can improve the noise shaping effect and the output power of the oscillator when the oscillator is in the current limited regime. In today's CMOS process, the Q factor of inductor is still worse than the capacitor or varactor [20,21]. Therefore, enhancing the Q factor of inductor is quite an effective solution to directly improve the phase noise. In addition to high Q factor, by making I_{bias} as large as is allowed or design for power dissipation specifications, and using minimum g_m of MOSFETs to satisfy start-up condition will also reduce the phase noise.

D. Circuit design and Layout

The design of the oscillator is based on the principle of a negative transconductance ($-g_m$) oscillator theory. A cross-coupled CMOS differential topology was chosen as the preferred topology owing to its low phase noise performance. VCOs are generally designed for minimum phase noise under constraints of dc power dissipation, tuning range, output voltage swing and die area. The dc power dissipation is given by

$$V_{supply} I_{bias} = P_{dissipation\ max} \quad \text{... (18)}$$

The differential pair thus can be modelled as a current source switching between and in parallel with a resistance–inductance–capacitance *(RLC)* tank. At the frequency of resonance, the admittances of the and cancel, leaving harmonics of the input current are strongly attenuated by the *LC* tank, leaving the fundamental component of the input current to induce a differential voltage swing of amplitude acrossthe tank if one assumes a rectangular current waveform. At high frequencies, the current waveform may be approximated more closely by a sinusoid due to finite switching time and limited gain. In such cases, the tank amplitude can be better approximated as,

$$V_{tank}\ I_{bias} R_p \quad \text{... (19)}$$

where $R_p = Q_L \omega_o L$ and V_{tank} is the single-ended peak-to-peak voltage swing at either the + or − output node of the VCO before any output buffering. This mode of operation is referred to as the

current-limited regime of operation since, in this regime, the tank amplitude is solely determined by the tail-current source and the tank resistance. In order to increase the voltage swing V_{tank} the bias current I_{bias} is set to an appropriate value, which is found to be 2.8 mA after iterations. The output amplitude of the CMOS LC oscillator is normally limited at the supply voltage. In this proposed scheme the capacitor between the source and gate of the NMOS transistors allows the NMOS transistors to clip the oscillator output voltage below ground potential. Since this capacitor is between the source and drain of the PMOS transistors, it allows the PMOS transistors to clip the oscillator output above the supply voltage.

The NMOS transistors are biased and laid out such that the required g_m is obtained to overcome all losses including those of the tank and the transistors themselves. The primary goal in the design of the oscillator is to size (design) the active devices to overcome the losses associated with the tank parallel resistance, *Rp*. The losses associated with the tank inductance (*L* = 2.1 nH) and capacitance (*C*= 2.09 pF) can be represented by the parallel resistance, *Rp* = 150Ù (obtained from inductor and varactor) design simulations. Active devices were sized to compensate for the losses associated with the tank parallel resistance, *Rp*. In order to enable sustained oscillations, it is imperative that the negative trans-conductance associated with the active devices (NMOS and PMOS transistor pairs) compensate for tank losses, hence the condition:

$$g_m \geq 6.67 \text{ mS} \quad \text{... (20)}$$

To ensure the occurrence of oscillations, a start-up safety factor of 3 was chosen. The resulting value of g_m is approximately equal to 10 mS. The negative trans-conductance of the parallel cross-coupled pair is given by the relation:

$$g_m = \frac{g_{mn} + g_{mp}}{2} \quad \text{... (21)}$$

where g_{mn} and g_{mp} is the trans-conductance associated with the NMOS and PMOS transistors, respectively. In order to maintain the symmetry of the oscillator outputs Gmn should be equal to Gmp, and in the current design, g_{mn}= g_{mp} = 10 mS. The MOS devices are sized, i.e., the W/L ratio of the NMOS (M1, M2) and PMOS (M3, M4) devices constituting the -g_m core are computed using the equation (5).

Table 1. Design Parameters

Parameter		Design Values
MOS Transistors	M_3	10.5 µ *m*/0.6 *um N*= 50
	M_4	10.5 µ *m*/0.6 *um N*= 50
	M_1	6 µ *m*/0.6 *um N*= 30
	M_2	6 µ *m*/0.6 *um N*= 30
L_P		*0.61 nH*
Micro Scale varactor		9 pF
C_1		10 %F
I_{bias}		2.8 mA
R_P		150 Ω
g_m		= 6.67 mS + (safety factor 1.5)

Layout of the proposed VCO is designed using a 90nm CMOS process in Microwind environment. The chip layout is illustrated in Fig 5. The CMOS section of the VCO structure is symmetrical. The layout area of the VCO is 320 *um*×380 *um*, including the bonding pads. The distance between the components is minimized in order to reduce the phase noise, and the layout is made as symmetrical and compact as possible to ensure differential operation and reduce parasitic inductance or capacitance.

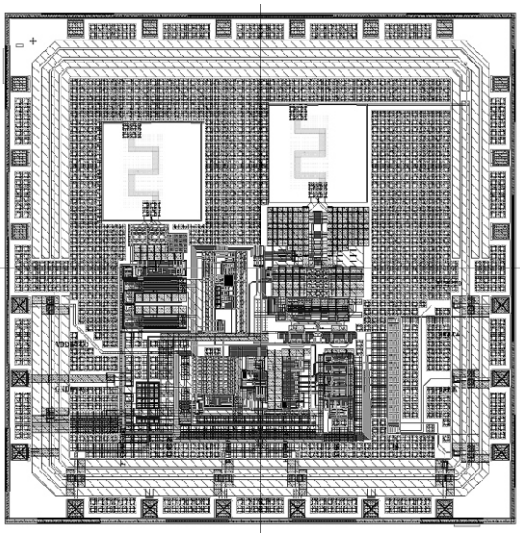

Fig. 5. Layout of the VCO

IV. PERFORMANCE ANALYSIS

The time referenced oscillation shown in Fig.6 and 7 is generated in Microwind environment using the cross coupled VCO topology. The oscillation frequency is measured as 2.40 GHz, with a 9 pF capacitor and 0.61nH inductance in the tank circuit. As shown in Fig.6, Simulation is performed with 0.6 volts power supply voltage and a current consumption of 0.461 mA in the core circuit. The output voltage oscillates above supply voltage and the maximum peak to peak voltage is 0.758 volts. As shown in Fig.7, Simulation is also performed with 0.3 volts power supply voltage and a current consumption of 36.361 μ A in the core circuit. The output voltage oscillates above supply voltage and the maximum peak to peak voltage is 0.347 volts.

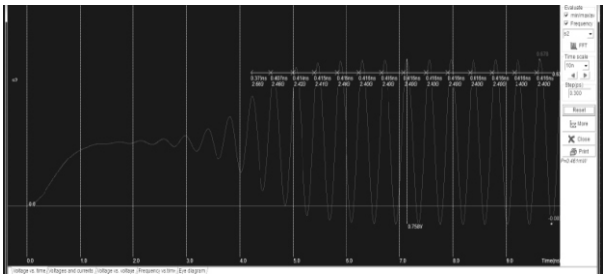

Fig. 6. Output oscillations of the layout shown in Fig 5 (VCO circuit shown in Fig 2) simulated with 0.6 V power supply

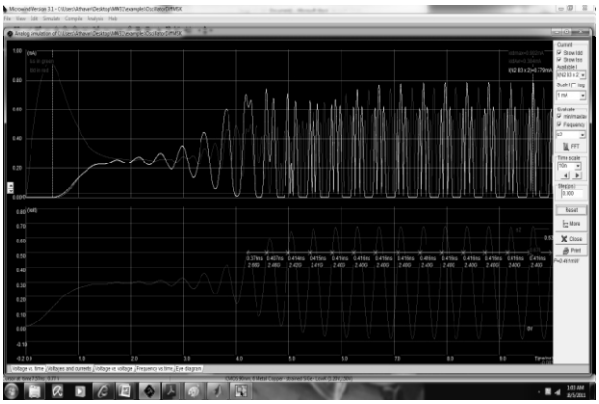

Fig. 7. Output oscillations of the layout shown in Fig 5 (VCO circuit shown in Fig 2) simulated with 0.3 V power supply

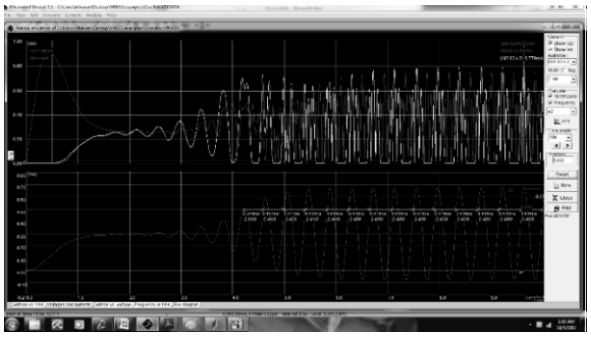

Fig. 8. Output voltage and current waveforms(PMOS) of VCO layout simulated using Microwind

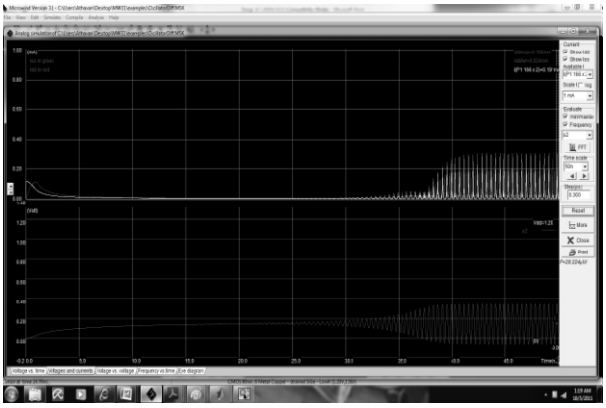

Fig. 9. Output voltage and current waveforms(PMOS) of VCO layout simulated using Microwind

Fig. 8 and Fig. 9 shows the output voltage and current waveforms of pMOS and nMOS transistors respectively. It is obvious form the graphs that the current consumption is proportional to the power supply voltage. The settling time of 0.6 and 0.3 volts oscillator is respectively 4.5 and 37 ns.

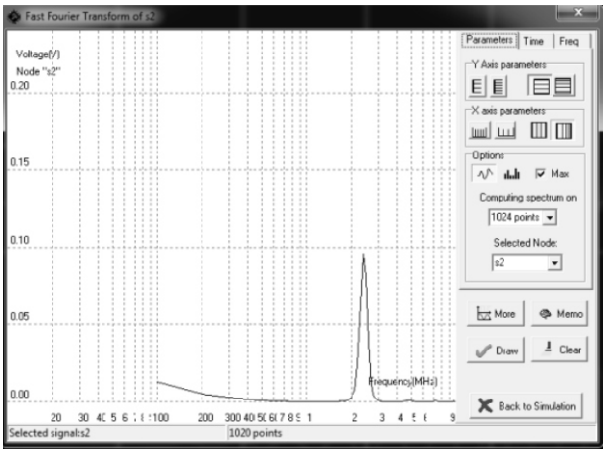

Fig. 10. Spectrum of VCO using 1024 point FFT

Fig.10 shows the spectrum of VCO with a center frequency of 2.4 GHz. The designed VCO exhibits a tuning frequency range of 780 MHz, with 2.4 GHz as center frequency which leads a tuning percentage of 32.5. The tuning range is even greater, since the micro scaled varactors have wide tuning range. Because of the trade off between the phase noise and the tuning frequency range, that the phase noise of the oscillator is inversely proportional to the tuning frequency range, the tuning frequency range is limited (this statement requires revision). The tank circuit impedance exhibits an inversely proportional relationship with the oscillation frequency. When the tank circuit impedance is lowered, the start up gain is reduced as well as output voltage swing. Hence the value of the tank circuit impedance is carefully chosen to avoid these issues. The quality factor of the resonant circuit at 2.4 GHz is calculated as 69, which provides a quality factor of 60 for the VCO at the same frequency. The gate-source and the drain source capacitance of the PMOS and NMOS transistors are measured between 0 to 3.5 fF.

V. CONCLUSION

A 2.4 GHz VCO is simulated and the results of the simulation are analysed. The results indicate VCO operation at a center frequency of 2.4 GHz with a predicted quality factor of 60. The chip size is $350\,\mu m \times 380\,\mu m$. The simulation predicts phase noise of -119 dBc/Hz at a power supply voltage of 0.6 V. The simulated oscillation amplitude swings above the maximum supply voltage and below the ground potential. The simulation operational conditions indicate that the device consumes ultra low power proportional to the supply voltage. Further the fabrication of the VCO is expected.

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REFERENCES

[1] Jan Crols and Michiel Steyaert, “CMOS Wireless Transceiver Design”, Springer, 1997.

[2] *Q. Gu, RF “System Design of Transceivers for Wireless Communications”, New York: Springer, 2005.*

[3] *To-Po Wang, Ren-Chieh Liu, Hong-Yeh Chang, Liang-Hung Lu, and Huei Wang*, “A 22-GHz Push-Push CMOS Oscillator Using Micromachined Inductors”, *IEEE Microwave and Wireless components letters, December, 2005,pp. 859-861*

[4] *S.-H. Tseng, Y.-J. Hung, Y.-Z. Juang, and M. S.-C. Lu, “*A 5.8-GHz VCO with CMOS-compatibleMEMS inductors*,”* Sensors Actuators A (Physical)*, vol. 139, pp. 187–193, Sep. 2007.*

[5] S. C. Li, H.-S. Kao, C.-P. Chen, and C.-C. Su, *“Low-power fully integrated and tunable CMOSRF wireless receiver for ISM band consumer applications,” IEEE Trans. Circuits Syst. I, Reg. Papers*,vol. 52, no. 9, pp. 1758–1766, Sep. 2005.

[6] J. Ryckaert, C. Desset, A. Fort, M. Badaroglu, V. De Heyn, P. Wambacq, G. Van der Plas, S. Donnay, B. Van Poucke, and B. Gyselinckx, “*Ultra-wide-band transmitter for low-power wireless body area networks: Design and evaluation,” IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2515–2525, Dec. 2005.

[7] W. Wang and H. C. Luong, “*A 0.8-V 4.9-mW 1.2-GHz CMOS fractional- N frequency synthesizer for UHF RFID readers*,” *IEEE Trans.Circuits Syst. I, Reg. Papers*, vol. 55, no. 9, pp. 2505–2513, Oct. 2008.

[8] H.-H. Hsieh and L.-H. Lu, “*A high-performance CMOS voltage-controlled oscillator for ultra-low-voltage operations*,” *IEEE Trans. Microw.Theory Techniques*, vol. 55, no. 3, pp. 467–473, Mar. 2007.

[9] C.-Y. Jeong and C. Yoo, “5-GHz low-phase noise CMOS quadrature VCO,” *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 11, pp. 609–611, Nov. 2006

[10] S.-H. Lee, Y.-H. Chuang, S.-L. Jang, and C.-C. Chen, “Low-phase noise Hartley differential CMOS voltage controlled oscillator,” *IEEE Microw. Wireless Compon. Lett.*, 17, no. 2, pp. 145–147, Feb. 2007.

[11] D.J. Young, and B.E. Boser, "*A micromachine-based RF low-noise voltage-controlled oscilator"*, in Proceedings IEEE Custom Integrated Circuits Conference, Santa Clara, CA, USA, May 5-8, 1997, pp. 431-434.

[12] D.J. Young, J.L. Tham, and B.E. Boser, "*A micromachine-based low phase-noise GHz voltage-controlled oscillator for wireless communications*", in 10th International Conference on Solid-State Sensors and Actuators (TRANSDUCERS '99) Digest of Technical Papers, Sendai, Japan, June 7-10, 1999, pp. 1386-1389.

[13] D.J. Young, B.E. Boser, V. Malba, and A.F. Bernhardt, "*A micromachined RF low phase noise voltage-controlled oscillator for wireless communications*", *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 11, no. 5, pp. 285- 300, Sept. 2001.

[14] B. Chi and B. Shi, "Integrated 2.4 GHz CMOS quadrature VCO with symmetrical spiral inductors and differential varactors," in *IEEE RFICSymp.*, 2002, pp. 451–454.

[15] C.W.Jerry E.Z. Mona , "*CMOS Micromachined Inductors With Structure Supports for RF Mixer Matching Networks" IEEE electron device letters*, November 2008, vol. 29, no. 11,PP.1209-1211

[16] N. Troedsson and H. Sjolamd, "*An ultra low voltage 2.4 GHz CMOS VCO*," in *IEEE Radio Wireless Conf.*, Aug. 2002, pp. 205–208.

[17] H. Wang, "*Oscillator circuit having maximized signal power and reduced phase noise*," U.S. Patent 6 229 406, May 8, 2001.

[18] Hseih-Hung Hseih, Liang-Hung Lu, "A High Performance CMOS Voltage Controlled Oscillator For Ultra-Low-Voltage Operations", IEEE Transactions on Microwave theory and Techniques, pp. 467-473, Vol no55, No3 ,2007

[19] R. Sujiang and H. C. Luong, "A 1V 4 GHz-and-10 GHztransformer-based dual-band quadrature VCO in 0.18 ìmCMOS," *Custom Integrated Circuits conference,* pp. 817-820, Sept. 2007.

[20] Itoh, N., Masuoka, H., Fukase, S., Hirashiki, K., and Nagata, M.'*Twisted inductor VCO for suppressing on-chip interferences'*. IEEE Proc. Asia-Pacific Microwave Conf. (APMC), Bangkok, Thailand, December 2007, pp. 1–4

[21] Poon, A., Chang, A., Samavati, H., and Wong, S.S.: 'Reduction of inductive crosstalk using quadrupole inductors', IEEE J. Solid-State Circuits, 2009, 44, (6), pp. 1756–1764

[22] B.S.Sreeja, and S.Radha, "Design and Modeling of a Wide Tuning Range, High Q, *Low Supply Voltage MEMS Based Tunable Capacitor for Wireless Communication Applications,* International Conference on MEMS NANO, and Smart Systems (ICMENS 2010), IEEE,

[23] B.S.Sreeja, and S.Radha, "*Design and simulation of a wide tuning range, high q, low supply voltage MEMS/NEMS tunable capacitor for wireless communication applications,* National Conference on Nanomaterials (NCN-2010),

[24] B.S.Sreeja and S.Radha "Design and Characterization of Multi Wall Carbon Nanotube Bundle Based Inductor for Wireless Communication Applications", (ICONE 2011), IEEE

[25] Aleksander Dec, Ken Suyama, Micromachined Electro-Mechanically Tunable Capacitors and Their Applications to RF IC's Ieee Transactions On Microwave Theory And Techniques, Vol. 46, No. 12,