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Analytical Modeling of Nanoscale Double Gate FinFET Device

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Abstract

FinFET is a novel double-gate device structure for future device design, modeling and circuit simulation purposes. FinFET have high-performance and low leakage, fully depleted silicon-on-insulator (FDSOI) device, which have been demonstrated down to 15 nm gate length and are relatively simple to fabricate, which can be scaled to gate length below 10 nm. In this paper the modeling of potential and current is carried out. Further the theoretical aspects of the series resistance, reliability issues, process variation effects and device scaling limits are also described for this device.

Key words : MOSFET, FinFET, Device Modeling, reliability issues

I. INTRODUCTION

The scaling of CMOS technology over the past several decades has resulted in continual improvements in integrated-circuit performance and cost per function. However, the scaling of conventional CMOS devices significantly beyond the 90-nm technology node will be challenging, due to limitations such as subthreshold leakage and gate-dielectric leakage [1]. To overcome some of the problems associated with planar CMOS device scaling, advanced MOSFET structures such as the double-gate FinFET device have been explored. These structures enable more aggressive device scaling because of their ability to control short-channel effects more effectively. Compared to a single-gate ultrathin-body device, the double-gate FinFET device is more electro-statically robust because two gates are used to control the channel, thus allowing for additional gate length scaling. Although double-gate transistors have been studied for quite some time, their adoption has been hindered by the complexity of their fabrication process [1, 5]. Recently, however, a more practical double-gate structure, the FinFET, was developed, with a process flow similar to that of conventional SOI CMOS processes [3]. According to Brew's scaling theory [4], the channel doping concentration in bulk MOSFETs should be continuously increased to suppress short-channel. Unfortunately, such a heavy doping concentration degrades device performance due to decreased mobility, increased junction capacitance, and increased junction leakage. Conventional bulk CMOS devices require aggressive gate oxide scaling, which increases the gate oxide leakage current, and ultra-shallow S/D (source/ drain) junctions to suppress short-channel effects. Alternative device structures are considered to circumvent these difficulties and continue to scale MOSFET gate lengths.

II. OVERVIEW OF 3D FINFET

Fig. 1. (a) shows 3D view and cross-section of FinFET. The gate 'wraps' over the thin Si Fin, yielding a quasi-planar symmetrical Double-Date MOSFET with two inversion channels that are beneficially charge-coupled. The FinFET is a symmetric double-gate structure. This means that both the front and back gates have the same work function and are tied to the same bias, so the two surface channels turn on at the same time.

The key challenges in the manufacture of double-gate devices are [6]:

(a) Self-alignment of the two gates,

(b) Formation of an ultra-thin silicon film.

Fig. 1. b depicts the geometry of the FinFET. The fin is a narrow channel of silicon patterned on an SOI wafer. The gate wraps around the fin on three faces. The top insulator (nitride) is usually thicker than the side insulators (oxide), hence the device has effectively two channels. The thickness of the fin (W_{fin}) represents the body thickness (t_{Si}) of the double-gate structure, while its height (H_{fin}) represents the channel width [6].

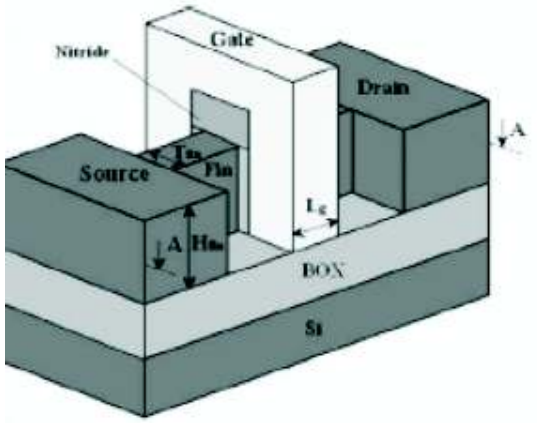

Fig 1. a. Overview of 3D FinFET

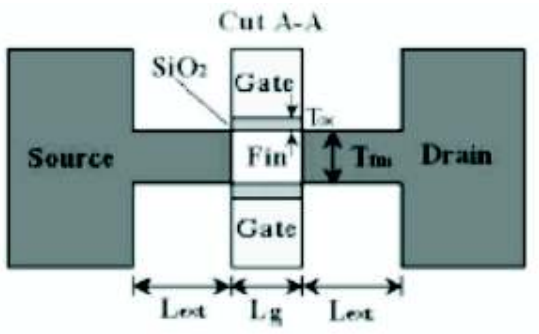

Fig. 1. b. Cross section of 2D FinFET

Series resistance

As the fin width is reduced, the parasitic series resistance in the source and drain increases. If the gate is misaligned to the source and drain pads, the output characteristics can be changed significantly. A selective *Ge* deposition process was proposed to alleviate the effect of misalignment and to reduce the series resistance [15]. The use of *Ge* is attractive because it is a low temperature process, which is important for future integration with high-K gate dielectrics and metal gates. Furthermore, *Ge* provides an in-situ cleaning effect because GeH4 can remove native oxide. On-current was enhanced to *28%* with selective *Ge* raised S/D process [15]. For further reduction of series resistance, metal germanide such as nickel-germanide can be attractive [2].

Reliability

It is timely to investigate reliability of FD-SOI CMOS FinFETs. For suppression of short-channel effects, the fin width is as narrow as possible. However, it can be a big concern that the extremely narrow fin width would be desirable in the device reliability point of view. Thus, DC hot-carrier tests were performed to evaluate device reliability for various device dimensions. In the thicker body case, hot electrons are more strongly driven towards the by the 2D curvature of the potential. Thus, hot-carrier immunity is improved by thinning the body of a double-gate MOSFET, which also improves short-channel effects [2], [9].

Parameters

A basic structure of FinFET is shown in Figure 2, which describes the different parameters used for the modeling. The critical geometrical parameters of FinFET are shown. Also the definition of these parameters described in the MOS control box as used in the setup of analytical and numerical modeling.

L_{gate}: physical gate length of FinFET, H_{fin}: height of silicon fin, defined by the distance between top gate and buried oxides, T_{fin}: thickness of silicon fin, defined by the distance between front and back gate oxides, L_{eff}: effective channel length of FinFET is estimated by the metallurgical junction for abrupt junctions, W: geometrical channel width defined as

$$W = 2 * H_{fin} + T_{fin}.$$

t_{oxf}: oxide thickness of the front gate;
t_{oxb}: oxide thickness of the back gate;

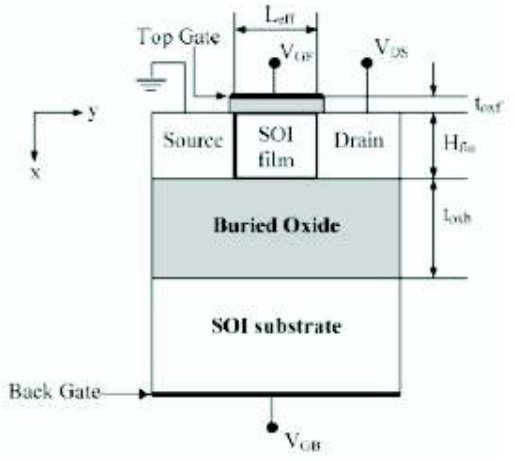

Fig. 2. Cross-sectional view of FinFET along the channel Length [7].

When Tfin is much larger than Hfin or when top gate oxide is much thinner than the front and back oxides, FinFET can be approximately treated as single-gate fully depleted SOI MOSFET (FDFET) as long as the silicon fin remains fully depleted. On the other hand, when Hfin is much larger than Tfin or top gate oxide is much thicker than the front and back oxides, FinFET can be approximately treated as DGFET. The two limits of FinFET, FDFET and DGFET, are widely studied and well understood, but in the regime where both fin height and fin thickness have control over SCE, the dependence of SCE on device dimensions is not well characterized. In order to establish the functional expressions of potential, analytical solution of 3D Laplace equation is used to derive the design equations for the subthreshold behavior of FinFET. Based on the 3D electrostatic potential distribution in the subthreshold region, potential modeling is done [7].

III. POTENTIAL MODELING

Electrostatic Potential in sub-threshold region can be describe by 3D Laplace equation [13].

$$\frac{\partial^2\psi}{\partial x^2}+\frac{\partial^2\psi}{\partial y^2}+\frac{\partial^2\psi}{\partial z^2}=0 \qquad (1)$$

The six boundary conditions are set by the top gate, front gate, back gate, source, and drain and buried oxide Fig. 1. The buried oxide is assumed to be thick enough that any finite potential across the buried oxide leads to a negligible electric field. The boundaries between gate oxide and silicon fin are eliminated by replacing the physical dimensions with effective dimensions [8].

Boundary conditions

Top gate:

$$\psi\big|_{z=H_{fin}}=V_g-V_{fb}$$

Bottom gate:

$$\psi\big|_{z=-H_{fin}}=V_g-V_{fb}$$

Front gate:

$$\psi\big|_{x=T_{fin}}=V_g-V_{fb}$$

Back gate:

$$\psi\big|_{x=0}=V_g-V_{fb}$$

Source side:

$$\psi\big|_{y=0}=-\phi_{ms}$$

Drain side:

$$\psi\big|_{y=L_{eff}}=-\phi_{ms}+V_{ds} \qquad (2.a)$$

Here ϕ_{ms} is the work function difference of S/D to the channel, V_{fb} is the flat band voltage. Superposition principle can be applied to solve the 3-D linear Laplace's equation and the total potential is the sum of the potential at top gate, front gate, back gate, source and drain potential. The expression for the total potential at different boundaries is as follows [13], [15].

$$\psi=\psi_{tg}+\psi_{fg}+\psi_{bg}+\psi_{s}+\psi_{d} \qquad (2.b)$$

The potential expressions for the individual gate at different boundary conditions are given in Appendix A. The simulation results of potential with Vds and Vgs are shown in Fig. 3. and Fig. 4. respectively.

IV. CURRENT MODELING

In this section the current modeling of the Double-Gate FinFET Electrostatics is explained. The modeling of the top gate in the first order will just be an addition of a transistor, which is the same as a planar MOSFET, with the width of the Fin defining the width of the planar MOSFET. Thus for simplicity, we derive the current equations for a DG-FinFET as [10].

$$I_{ds}=\mu_{eff}W_{fin}q_I\frac{dV_{ch}}{dy} \qquad (3)$$

where $\mu_{eff}=\dfrac{\mu_s}{1+\mu_S\left(\dfrac{V_{ds}}{v_{\max}L_{fff}}\right)}$

Where q_I is inversion layer charge, V_{ch} is the quasi Fermi potential in the channel, μ_{eff} is effective surface mobility and the current flows in the positive y direction, W_{fun} is the width of FinFET, The value of v_{max} is $5x10^6 m/s$ [16]. The inversion charge in the channel can be expressed as,

$$q_I=n_1\log[1+\exp\left(\frac{(V_{G1}+(n_1-1)V_{G2}-V_T)}{n_1}-V_{ch}\right) \qquad (4)$$

Where V_{G1} and V_{G2} are voltage applied at front and back gate respectively. An expression for current in term of charge is obtained as below [14]:

$$I_{ds}=\mu_{eff}W\frac{(1+q_I/n_1)dq_I}{dy} \qquad (5)$$

Where $n_1=1+\left(\dfrac{C_{si}C_{ox2}}{C_{ox1}(C_{si}+C_{ox2})}\right)$

After integrating eq (5) from source to drain, the drain current is given by

$$I_{ds}=\frac{\mu_{eff}W}{L_{eff}}\left(\frac{q_S^2-q_D^2}{2n_1}+(q_S-q_D)\right) \qquad (6)$$

Where q_S and q_D are the normalized charge at source and drain respectively. To get analytical solution of charge at source and drain replace the V_{ch} with source and drain voltage respectively in equation of inversion charge [11], [14].

$$q_S=n_1\log[1+\exp\left(\frac{(V_{G1}+(n_1-1)V_{G2}-V_T)}{n_1}-V_S\right)$$

$$q_D=n_1\log[1+\exp\left(\frac{(V_{G1}+(n_1-1)V_{G2}-V_T)}{n_1}-V_{DS}\right)$$

V_T is the threshold voltage, which is calculated from the following expression:

$$V_T=2V_{FB}+2\phi_B+qN_AW_{fin}\left(\frac{C_{si}+C_{ox}}{C_{si}C_{ox}}\right) \qquad (7)$$

$$V_T = 2V_{FB} + 2\phi_B + qN_A W_{fin}\left(\frac{C_{si}+C_{ox}}{C_{si}C_{ox}}\right)$$

In this equation V_{FB} is the flat band voltage, ϕ_B is the Fermi potential, W_{fun} is the width of FinFET device.

V. RESULTS

In this paper the analytical modeling of potential and drain current for FinFET has been carried out for the device parameters Leff=60 nm, Heff =60 nm, Teff =20 nm, Vds=0.8 V, Vgs=0.2 V. Fig. 3 and Fig. 4 show the variation of potential with the distance along the channel length. at Vds = 0 V & 0.8 V respectively. Fig. 5 shows the variation of drain current with Vds, at Vgs=0.2 V. Fig. 6 shows the variation of Drain current with Vgs, at Vds=0.8 V.

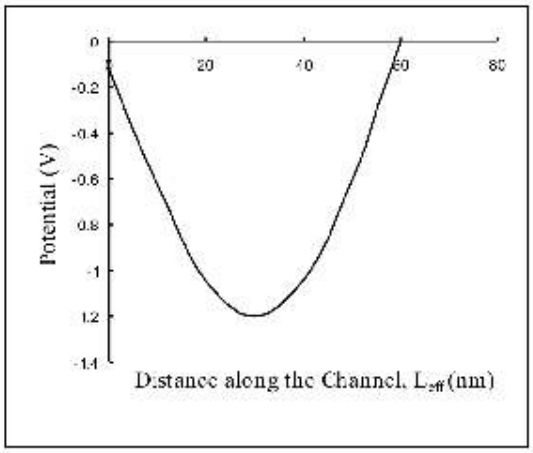

Fig. 3. Potential profile of FinFET at V_{ds}=0V

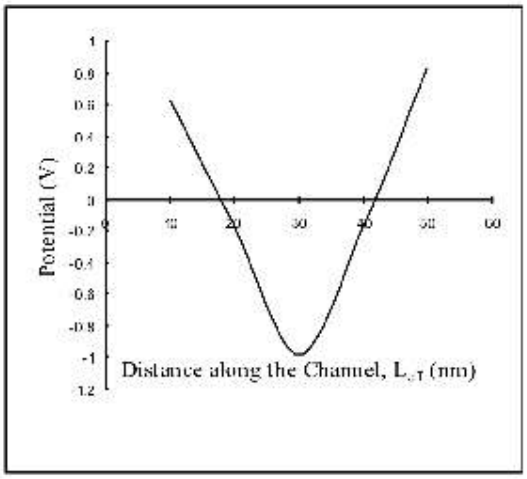

Fig. 4. Potential profile of FinFET at V_{ds}=0.8V

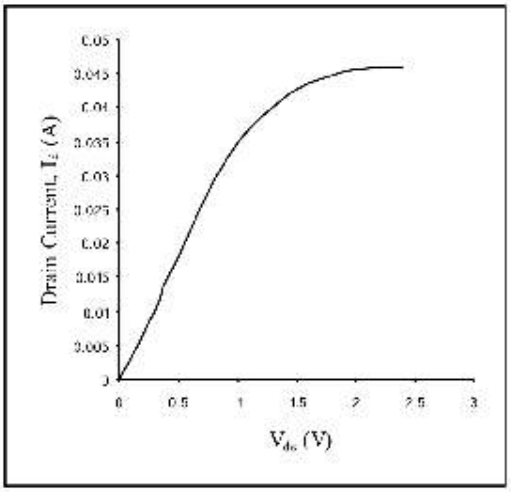

Fig. 5. Variation of drain current with V_{ds} (V)

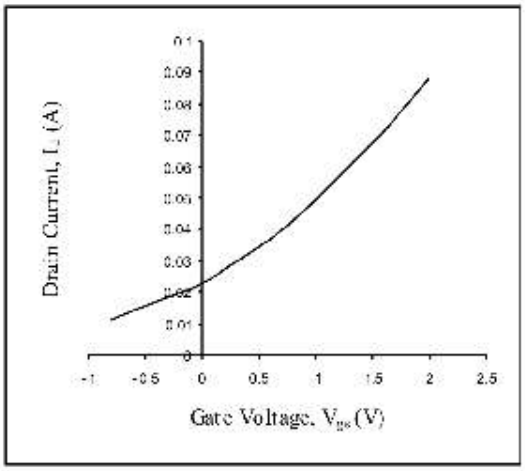

Fig. 6. Variation of drain current with $V_{gs=}$ (V)

VI. CONCLUSION

A FinFET is novel double-gate device structure demonstrated for sub-10nm device scaling. Key issues including FinFET device structure, Design parameters, potential modeling, current modeling, series resistance, reliability issues, process variation effects and device scaling limit are discussed. While a number of challenges remain to be overcome. Simulation results for potential profile of FinFET obtained along the channel distance at V_{ds}=0 V & 0.8 V. The drain current variation with V_{ds} at 0.2 V gate voltage and with V_{gs} at 0.8 V drain voltage is obtained for FinFET is similar to bulk MOSFET. The double-gate FinFET will lead the further device scaling. This model would be useful for the device as well as design engineers to fabricate the nanoscale FinFETs device and to simulate the circuits for circuit simulation purposes for future technology.

Appendix a potential modeling

$$\psi_{fg} = \sum_{m=1,n=1}^{\infty} \frac{16(V_g - V_{fb})}{(2n-1)(2m-1)\pi^2} \sin\left(\frac{(2m-1)\pi}{L_{eff}} y\right) \sin\left(\frac{(2n-1)\pi}{T_{eff}} x\right) \frac{\cosh\left(\frac{k_z\pi}{H_{eff}} z\right)}{\cosh(k_z\pi)}$$

$$\psi_{fg} = \sum_{m=1,n=1}^{\infty} \frac{16(V_g - V_{fb})(-1)^{n+1}}{(2n-1)(2m-1)\pi^2} \sin\left(\frac{(2m-1)\pi}{L_{eff}} y\right) \cos\left(\frac{(2n-1)\pi}{2H_{eff}} z\right) \frac{\sinh\left(\frac{k_x\pi}{T_{eff}} x\right)}{\sinh(k_x\pi)}$$

$$\psi_{bg} = \sum_{m=1,n=1}^{\infty} \frac{16(V_g - V_{fb})(-1)^{n+1}}{(2n-1)(2m-1)\pi^2} \sin\left(\frac{(2m-1)\pi}{L_{eff}} y\right) \cos\left(\frac{(2n-1)\pi}{2H_{eff}} z\right) \frac{\sinh\left(\frac{k_x\pi}{T_{eff}} (T_{eff} - x)\right)}{\sinh(k_x\pi)}$$

$$\psi_s = \sum_{m=1,n=1}^{\infty} \frac{-16\phi_{ms}(-1)^{n+1}}{(2n-1)(2m-1)\pi^2} \sin\left(\frac{(2m-1)\pi}{T_{eff}} x\right) \cos\left(\frac{(2n-1)\pi}{2H_{eff}} z\right) \frac{\sinh\left(\frac{k_y\pi}{L_{eff}} (L_{eff} - y)\right)}{\sinh(k_y\pi)}$$

$$\psi_d = \sum_{m=1,n=1}^{\infty} \frac{-16(\phi_{ms} - V_{ds})(-1)^{n+1}}{(2n-1)(2m-1)\pi^2} \sin\left(\frac{(2m-1)\pi}{T_{eff}} x\right) \cos\left(\frac{(2n-1)\pi}{2H_{eff}} z\right) \frac{\sinh\left(\frac{k_y\pi}{L_{eff}} y\right)}{\sinh(k_y\pi)}$$

$$k_x = \sqrt{\left(\frac{2m-1}{L_{eff}}\right)^2 + \left(\frac{2n-1}{2H_{eff}}\right)^2} \times T_{eff}$$

$$k_y = \sqrt{\left(\frac{2m-1}{T_{eff}}\right)^2 + \left(\frac{2n-1}{2H_{eff}}\right)^2} \times L_{eff}$$

$$k_z = \sqrt{\left(\frac{2n-1}{T_{eff}}\right)^2 + \left(\frac{2m-1}{2H_{eff}}\right)^2} \times H_{eff}$$

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