

## TECHNIQUES FOR GLITCH POWER REDUCTION IN CMOS VLSI CIRCUITS

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### Abstract

The dynamic power dissipation is the dominant source of power dissipation in CMOS circuits. It is directly related to the number of signal transitions and glitches. The glitches occupy a considerable amount of power of the total power dissipation in CMOS circuits. This paper presents a survey of the different techniques used for decreasing the dynamic power by reduction of glitches. The advantages and limitations of these techniques are also discussed.

**Key words:** Glitches, CMOS circuits, low power, path balancing, gate sizing.

### I. INTRODUCTION

Power dissipation has emerged as an important design parameter in the design of microelectronic circuits, especially in portable computing and personal communication applications. The total power consumed by a CMOS circuit consists of four components: functional switching, hazards or glitches, short circuit and leakage [1, 2, 3, 8]. Functional switching power is an important component as it corresponds to the desired logic state. Hazard or glitch power is consumed by the transients before a steady logic state is achieved. These glitches consume about 20–40% of total power even though they do not affect the operation of the system. For a  $16 \times 16$  bit multiplier with a logic depth of 30, glitches consume as much as 67% of the total power [3].

Fig 1. shows the hazards which are due to the differing delays of logic cells. In Fig. 1(a), the output returns to the logic 1 state after completion of a transient pulse of width  $w$ . This pulse is called static hazard. In Fig. 1(b), the output of the AND gate has a logic value changing from 0 to 1. The transient consists of three edges, two rising and one falling, which is known as the dynamic hazard. The arrival times of signals at the inputs of gate could be quite different, which lead to multiple transitions at the output before it settles to the correct logic value.

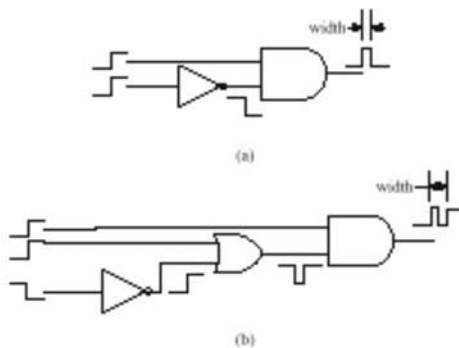


Fig. 1 (a) Static Hazard, (b) Dynamic Hazard.

Since a large amount of power is wasted due to glitches, the reduction of glitches and glitch power is the topic of this paper. Different techniques on reducing glitches are postulated in recent papers [7–10, 12]. Some of the important techniques are balanced delay, hazard filtering, transistor sizing, gate sizing and linear programming. This paper intends to describe the different techniques used for eliminating glitches and glitch power in VLSI circuits.

The rest of the paper is organized as follows. In section 2, the balanced delay method is discussed, the section 3 presents the hazard filtering for glitch reduction, the sections 4 and 5 explain the gate sizing and transistor sizing method, the linear programming technique is shown in section 6, and the section 7 concludes the paper.

### II. BALANCED DELAY

In the balanced delay or path balancing method, the hazards are eliminated by equalizing the delays of multi-path signals arriving at the gate, either by inserting delay buffers in small delay path or by using a tree like logic structure [4, 7, 12]. When a signal fans out, its delay affects several paths and balancing requires the insertion of delay buffers on selected fan out branches. Toshiyuki Sakuta et al. [7] discussed the reduction of glitch power in the Wallace tree multiplier and array multiplier by the balanced delay method. Experimental results show that 6.5% and 36% of power saving were attained in the Wallace tree and array multiplier respectively. In Kim et al. [12], the author presents an algorithm that maximizes the path balancing and minimizes load capacitance at the same time. Experimental results show 61.5% glitch reduction and 30.4% power reduction without increasing the critical path delay. The advantage of this method is that the overall delay of the circuit does not increase even if buffers are inserted.

### III. HAZARD FILTERING

An alternative to the balanced delay method is hazard filtering. In this method, the width of a pulse is less than the inertial delay of the gate and the pulse will be suppressed (or) filtered out by the gate. D. Agrawal [8] discussed hazard filtering by adjusting the inertial delay to be greater than the differential path delay of the arriving inputs at the gate and in this way glitches can be eliminated. Differential path delay ( $w$ ) is computed for each gate and the inertial delay can be reduced to the least permissible value. Once inertial delays are changed, the differential path delays are recomputed. Adjustment of delay for hazard suppression is performed from inputs to outputs. Fig 2 shows the difference between the hazard filtering and balanced delay method. In Ref. [9], hazard filtering is applied to the circuit level design using a linear programming method to find the minimum inertial delay for each gate. Experimental results show that a 4-bit ALU consumes only 53% peak power after the optimization. The advantage of this method is that delay buffers are not required, but the limitation is that it increases the overall delay.

### IV. GATE SIZING

In the gate sizing method, the logic gates in a circuit are modeled as an equivalent inverter. Then sizing optimization on the modeled circuit is carried out with equivalent inverter in the place of real gates [10]. The number of parameters to be determined is far less than in case of transistor sizing, which make it an easier problem than the transistor sizing problem. The gate size is allowed to vary in a continuous manner between a

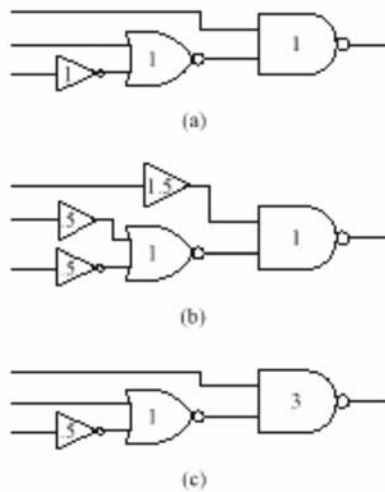


Fig. 2 (a) Original Circuit, (b) Balanced Delay Method, (c) Hazard Filtering Method.

minimum and maximum size. The gate sizing technique suffers from the non linearity problem of the delay model. So a nonlinear programming solver [11] may be used for solving the problem. T. Raja et al. [22] described that the complexity of these techniques limit the maximum size of circuit that can be analyzed and optimality of the solution. Sungja Kim et al. [12] developed an algorithm for gate sizing in such a way to reduce the glitch power dissipation in the CMOS circuit. This algorithm has been tested on LG Synth91 benchmark circuits and 61.5% of glitches are reduced experimentally.

### V. TRANSISTOR SIZING

This technique is similar to the gate sizing where size of transistor is changed. In this method the glitches are eliminated by the transistor sizing under delay assignment [13–17]. Transistor sizing is the operation of enlarging (or reducing) the width of the channel of a transistor. It is an effective technique to improve the delay of a CMOS circuit. When the width of the channel is increased, the current drive capability of the transistor increases which reduces the signal rise or fall times at the gate output.

Transistor sizing problem is analyzed using the convex optimization [13] technique. Borach et al. [14, 15] applied the transistor sizing technique in low power circuits in which the transistor size is derived for both capacitive and short circuit power. Recently Wroblewski et al. [18, 19] described that the balanced delay was considered in transistor sizing together with minimizing of total capacitance and short circuit power. The solution is formulated as a multiobjective optimization where path delay difference and power consuming are the design objective. An experimental result shows that the power reduction for a  $16 \times 16$  multiplier is 45.6%. The advantage of this method is that it does not add buffer. However, it suffers from increased non linearity delay model.

### VI. LINEAR PROGRAM

Another method for reducing glitches is delay assignment using linear programming technique [9, 20–23]. A linear program determines a set of variables such that an objective is minimized under given constraints. In this method the circuit is formulated as a linear program and delays of gates are treated as variable. Agrawal et al. [9] proposed a linear programming for digital circuits to find the minimum transient energy. In this paper, the linear programming was incorporated with hazard filtering, to determine the delay assignment for each gate. A single gate inertial delay is associated with each gate. It has been shown that insertion of a delay buffer is required if the objective is to eliminate all glitches and control the overall delay.

Consider a gate with two inputs 1 and 2. The minimum transient energy (MTE) conditions for this gate ensures that the delay difference between path  $p_1$  and  $p_2$  arriving at input 1 and 2, respectively, is not greater than the inertial delay ( $d$ ) of the gate

$$\sum_{p_1\text{-path}} \text{gate delays} - \sum_{p_2\text{-path}} \text{gate delays} \leq d, \quad (1)$$

such a condition must be satisfied for all pair of path terminating at inputs of all gates. Thus if the sets  $p_1$  and  $p_2$  have  $k_1$  and  $k_2$  elements, respectively, then there are at least  $k_1$  and  $k_2$  constraints for that gate. As the level of gate increases  $k_1$  and  $k_2$  increase and hence the number of constraints for the gate increases exponentially with size of the circuit. Additional constraints are used to hold the overall circuit delay within limits,

$$\sum_{pi-po\text{ path}} \text{gate delays} \leq \text{max delay} \quad (2)$$

where max delay is a design parameter. To enforce the overall delay constraint the path enumeration method was used. As the constraints on various gates are not independent, further analysis is required to total the number of constraints. The improved linear constraint set (reduced constraint set) was proposed by Raja *et al.* [20] instead of path enumeration, which reduced the complexity of the constraints set from exponential to linear in circuit size. In this method they introduce two new variables for every gate, one for earliest time and the other for the most delayed time of arrival of signal at the output of gate. The difference of these variables is a timing window within which the various signals arrive at the gate. The main advantage of this technique is the linear size the complexity of the constraint set with the size of the circuit.

Raja *et al.* again [21] reduce dynamic power by redesigning the circuit which eliminates the buffer inserted into the circuit with least reduction in speed. In this method gates are designed with different input output delay along different I/O paths through the gate. Thus the gates consist of an inertial delay for the output and set of delays for the input. Linear programming technique is used to determine the optimal delay under the constraints of feasibility parameter and overall delays. Experimental results show up to an additional 24% power saving compared to a previous method [20]. The advantage of linear programming method is to solve any type of circuit using linear program solver. The problem with this technique is that the additionally inserted elements also consume power. Later Raja *et al.* [22] described a technique for reducing glitches using special gates known as Variable Input Delay (VID) gate where the delay through any input–output path can be manipulated without affecting the delays of the other path.

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## VII. CONCLUSION

We have surveyed the different techniques used for reducing glitch power in CMOS circuit: namely hazard filtering, path balancing, gate sizing, transistor sizing and linear programming. Every method has its advantages and disadvantages. The effect of variation in the supply voltage, optimization of routing and layout are not considered. A study of transistor sizing issues with scaling

of voltage and optimization of routing would be interesting future work for glitch reduction. Because of the growing demands from portable computing and communication devices, further analysis and optimization of power due to glitches are necessary for low power CMOS VLSI circuits.

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