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MODIFIED MULTIPLY-ACCUMULATE ARCHITECTURE WITH THE SWITCHING POWER SWIFTNESS IMPROVEMENT TECHNIQUE

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Abstract

This paper presents a 32-bit multiply-accumulator (MAC) architecture capable of supporting multiple precisions. The MAC architecture is multiplexing into the partial product generation and by inserting partial product in the carry chain of the reduction tree and the final carry-propagate adder. This Switching Power Swiftness Improvement Technique (SPSIT) has been applied on both the compression tree of the multipliers and the modified Booth Encoder to enlarge the power swiftness, for high-speed and low-power purposes. To filter out the spurious switching power of the MAC unit, there are two approaches, i.e., using registers and using AND gates, to assert the data signals of LP multipliers after the data transition has been proposed. The SPSIT approach leads to a 40% power consumption reduction and speed improvement when compared with the other power minimization technique. This is an example of "shared segmentation" in which the existing scalar structure is segmented and then shared between vector modes. The MAC is area efficient, which makes it suitable for high-performance processors and, possibly, dynamically reconfigurable processors.

Key words: High-speed arithmetic, data-path design, VLSI, MAC, multiply-accumulate, multiplier, vector, modified Booth, Wallace, signed, unsigned, integer, fixed-point.

I. INTRODUCTION

Low-power and low-energy VLSI circuits have become an important issue in today's consumer electronics. The number of embedded devices that must run with battery power or parasitic power continues to grow. The traditional approaches for designing these systems vary according to the need of low power design. Enhancing the processing performance and lowering down the power consumption of the circuit designs are undoubtedly having the challenges in low-power VLSI Design. The addition of multiply capabilities to processor architecture can provide significant boost in performance for low-power wireless multimedia and Digital Signal Processor (DSP) applications such as Fast Fourier Transform (FFT), Discrete Cosine Transform (DCT), quantization, and filtering. It is well known that the clamp-down approach of dynamic power which is the major part of total power dissipation may provide significant reduction in power consumption. This can be achieved by minimizing the switching capacitance.

The reduction of dynamic power consumption by minimizing the switched capacitance has been reported by many researchers [1-7]. Choi et al [1] proposed partially guarded computation (PGC) which divides the arithmetic units e.g., adders and multipliers into two parts, and turns off the unused part to minimize the power consumption. The reported results show that the PGC can reduce power consumption by 10% to 44% in an array multiplier with 30% to 36% area overheads in speech related applications. A 32-bit 2's complement adder equipping a dynamic-range determination (DRD) unit and a sign-extension unit was reported by Chen et al [2]. This design tends to reduce the power dissipation of conventional adders for multimedia applications. Later Chen et al [3] presented a multiplier using the DRD unit to select the input operand with a smaller effective dynamic range to yield the Booth codes and it saves 30% power dissipation than conventional ones. Benini et al [4] reported that the technique for glitching power minimization by replacing some existing gates with functionally equivalent ones that can be "frozen" by asserting a control signal. This saves 6.3% of total power dissipation since it operates in the layout-level environment which is tightly restricted. The double-switch circuit-block switch scheme capable of reducing power dissipation during down time by shortening the settling time after reactivation was proposed by Henzler [5]. Huang et [6] also presented the arithmetic details about the signal gating schemes and illustrates 10% to 45% power reduction for adders. The combination of the signal flow optimization (SFO), left-to-right leapfrog (LRLF) structure, and upper/lower split structure was incorporated in the design to optimize the array multipliers by Huang [8] and it is reported that the new approach can save about 20% power dissipation. Wen et al [9] reported that the turning off some columns in the multiplier array whenever their outputs are known can save 10% power consumption for random inputs.

In order to improve the performance, the architecture with accelerating multiplication is expected. In this paper, the Multiply-Accumulator unit with SPSI technique is

considered for improving performance in terms of low power consumption and hence the speed.

II. MODIFIED BOOTH MULTIPLIER

It is known that the bit- pair recoding is used to speed-up the multiplication process in the Booth's algorithm. In this technique, the Booth-recoded multiplier bits are grouped in pairs and then each pair is represented by its equivalent single bit multiplier reducing total number of multiplier bits to half. For example pair (+1 -1) is equivalent to the pair (0+1). That is, instead of adding - 1 time multiplication at shifted position i to +1 time the multiplicand at position +1 , the same result is obtained by adding +1 time multiplicand at position i. Similarly, (+10) is equivalent to (0+2), (-1 +1) is equivalent to (0 -1), and so on. By replacing pairs with their equivalents we can get bit-pair recoded multiplier. But instead of deriving bit- pair recoded multiplier from Booth recoded multiplier one can directly derive it from original multiplier. The bit- pair recoding or multiplier can be directly derived from Table 1. which shows the bit-pair code for all possible multiplier bit options.

Table 1. Bit-pair recoding scheme.

Multiplier bit-pair (i+1)	Multiplier bit-pair (i)	Multiplier bit-pair(i-1)	Bit-pair recoded multiplier bit at position (i)
0	0	0	0
0	0	1	+1
0	1	0	+1
0	1	1	+2
1	0	0	-2
1	0	1	-1
1	1	0	-1
1	1	1	0

E.g.: By referring the above table 1. The bit-pair code for a multiplier 0000000001101010 can be derived as follows

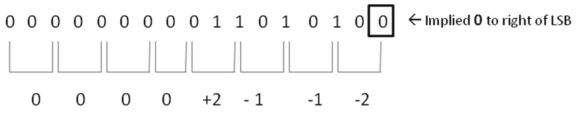

Fig. 1. Bit Pair Recoding of "006A"

Consider a Modified Booth Multiplication with two numbers "2AC9" and "006A". The above Fig. 1. Shows the Bit Pair Recoding of multiplier "006A". The recoded output 0000+2-1-1-2 has been considered as new multiplier and this will reduce the multiplication process into half of its original step, this lead to the reduction of power consumption by half. The modified booth multiplied partial products are represented by PP0, PP1, PP2, PP3…etc as shown in the below Fig. 2.

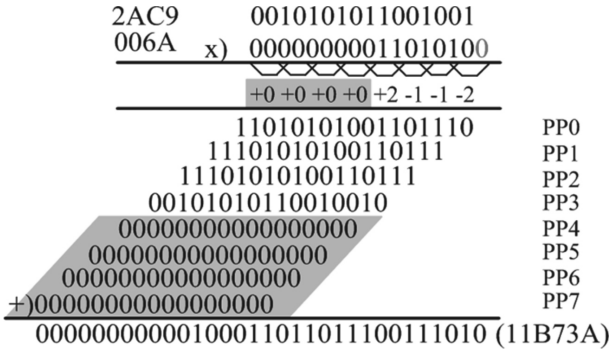

Fig. 2. Illustration of multiplication using Modified Booth Encoding.

The PP candidates are added using a SPSIT-equipped adder to get the final result. When an application such as fast Fourier transforms (FFT), discrete cosine transform (DCT), quantization, and filtering are concern multiplication is 16 bit and the speed of operation is depends up on the processor. For DSP applications the input data is sophisticated, at that time the multiplication process is split down to MSP and LSP. Then the operation has been carried out with the help of some latch to switch down some unwanted signals and transients power to get perfect output.

III. SWITCHING POWER SWIFTNESS IMPROVEMENT TECHNIQUE (SPSIT)

The implementation approaches of Switching Power Swiftness Improvement Technique (SPSIT) design concept and its application on a low-power (LP) MAC unit is described in this section. This SPSIT approach can be applied on both the compression tree of multipliers and the Modified Booth Encoder to enlarge the switching power swiftness.

To illustrate the influence of the spurious power signal transitions, five cases of a 16-bit addition are explored as an example below (shown in Fig. 3.)

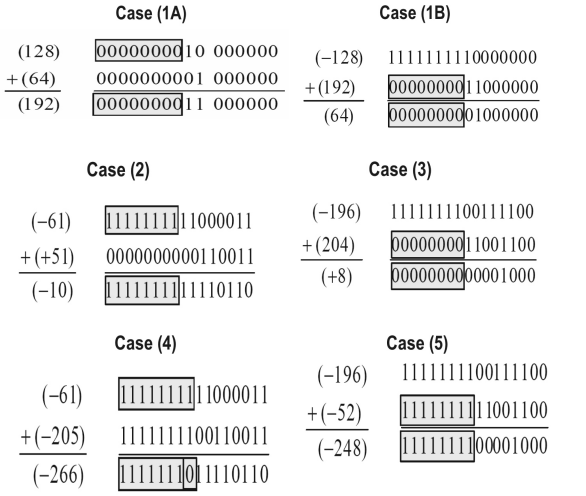

Fig.3. spurious power signal transition examples

The first case illustrates a transient state in which the illogical transitions of carry signals occur in the MSP though the final result of the MSP are unchanged. The second and third cases describe the situations of one negative operand adding another positive operand without and with carry from LSP, respectively. Moreover, the forth and fifth cases demonstrate the conditions of two negative operands addition without and with carry-in from LSP respectively. In those cases, the results of the MSP are predictable, therefore the computations in the MSP are useless and can be neglected.

Eliminating those spurious computations will not only save the power consumed inside the SPSIT MAC but also decrease the glitching noises which will affect the next arithmetic circuits. The MAC unit consists of different multiplier sections as in Fig.4. and each section is controlled by SPSIT. The main contribution of SPSIT is to exploring two implementing approaches and comparing their efficiency to get different material for the reduction of power and to increase the speed of operation. Fig.5. shows the simplified implementation approach for the addition /subtraction of two bit numbers.

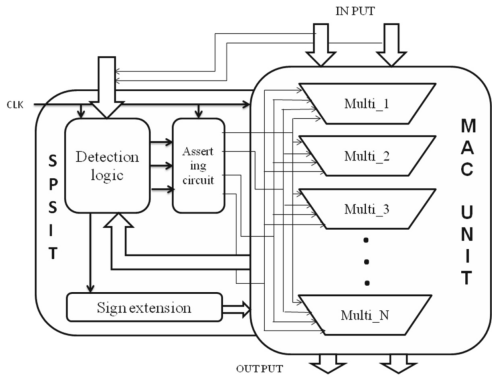

Fig.4. MAC unit with SPSIT

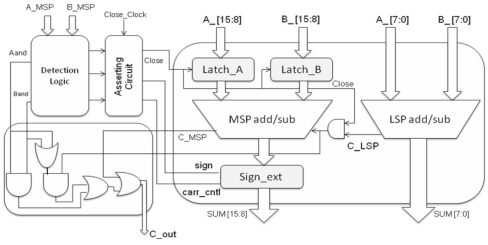

Fig. 5. Low-power adder/substractor example based on proposed SPSIT.

The adder/ subtractor are divided in to two parts. i.e., Most significant part (MSP) and Least significant part (LSP). The MSP of the original adder/subtractor is modified to include detection logic circuit, data controlling circuits (The data controlling circuits mainly consists of latch A and latch B),sign extension circuit and some glue logics for carry in and carry out signal.

A. Multiply-accumulate (mac) Architecture With Spsit

The block diagram of the vector MAC unit is shown in Fig. 6. The MAC unit consists of a Modified Booth Recoder Partial Product Generator (PPG), a Carry-Save Adder (CSA) Partial Product Reduction Tree (PPRT). The accumulator is fed into the MAC tree and only adds one extra stage of CSA asserting delay. The Switching Power Swiftness Improvement Technique (SPSIT), Which is carried out by a detection logic circuit, asserting circuit and a modified booth multiplier to increase the speed of multiplication operation into double by reducing the multiplication using a bit pair recoding scheme.

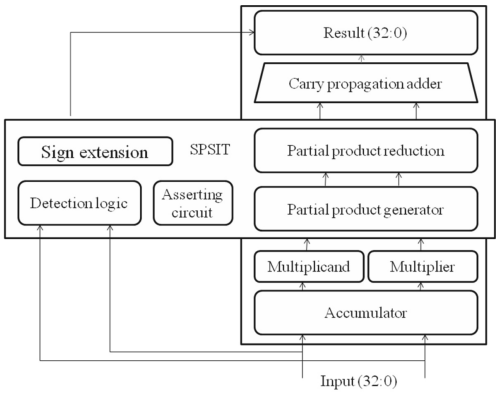

Fig. 6. MAC architecture with SPSIT.

B. Implementation of Mac Using Spsit

The low-power multiplier is designed by equipping the SPSIT on a tree multiplier unit. There are two distinguishing design considerations in designing the proposed multiplier and SPSIT, as listed in the following.

B.1 Applying The Spsit On The Mbe

In Fig. 2, the shadow denotes that the numbers in this part of Booth multiplication are all zero so that this part of the computations can be neglected. Saving those computations can significantly reduce the power consumption caused by the transient signals. According to the analysis of the multiplication the SPSIT-equipped modified-Booth encoder (MBE), this is controlled by a detection unit. The detection unit has one of the two operands as its input to decide whether the Booth encoder calculates redundant computations. As shown in Fig. 7, the latches can, respectively, freeze the inputs of MUX-4 to MUX-7 or only those of MUX-6 to MUX-7 when the PP4 to PP7 or the PP6 to PP7 are zero, to reduce the transition power dissipation. Such cases occur frequently in e.g., FFT/IFFT, DCT/IDCT, and Q/IQ which are adopted in encoding or decoding multimedia data.

B.2 Spsit On The Compression Tree

The proposed SPSIT-equipped multiplier is illustrated in Fig.7. The PP generator generates the candidates of the partial products, which are then selected according to the Booth encoding results of the operand B. Moreover, when the operand besides the Booth encoded one has a small absolute value, there are opportunities to reduce the spurious switching power dissipated in the compression tree. According to the redundancy analysis of the additions, we replace some of the adders in compression tree of the multiplier with the SPSIT - equipped adders, which are marked with oblique lines in Fig. 8. The bit-widths of the MSP and LSP of each SPSIT - equipped adder are also indicated in fraction values.

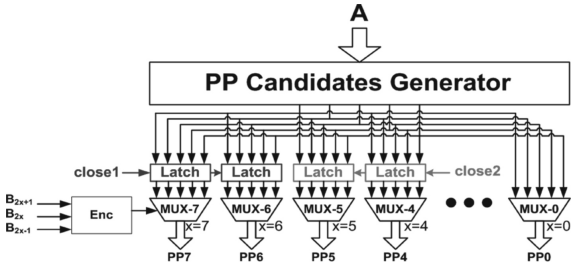

Fig. 7. SPSIT-equipped MBE

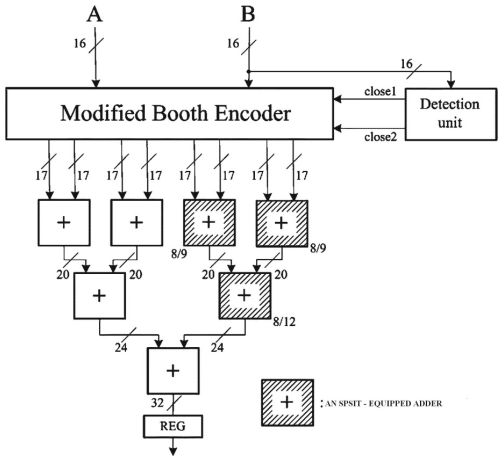

Fig. 8. SPSIT adder

C. Detection Logic Circuit Design

The detection logic circuit is used to detect the zero's present in the input of the multiplier. When we are using this low power multiplier for FFT, IDFT, DFT calculation, before the multiplication process we would identify the zeros in the input to effectively use SPSIT. Also detection logic circuit is act as isolation between the processor and the multiplier section. The output of detection logic circuit consists of three signals namely Close- this is used for to control the Latch, Carr.ctr- which is used to control the carry signals and Sign Extension- used to maintain the sign of the output as shown in Fig.9.

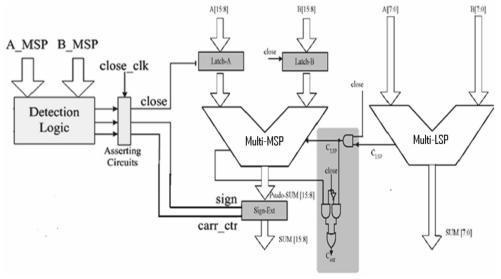

Fig.9. A Multiplier unit section with Detection Logic Circuit

A detection logic circuit design using register is as shown in the Fig.10. The shadow section indicates the registers used in this circuit for to control the latch, carry and sign ext. Again to clampdown the power consumption, the register is suppressed in to an AND gate to control the signal assertion. When speed is seriously concerned, this implementing approach enables an extremely high flexibility on adjusting the data asserting time of SPSIT equipped multipliers. Therefore, the SPSIT can benefit multipliers on both high speed and low power features.

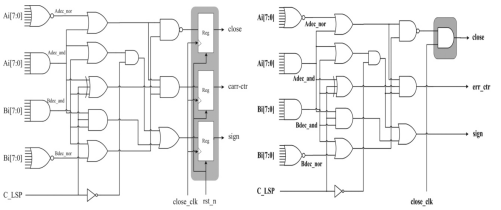

Fig. 10.. Detection logic circuits using registers and AND gate to assert the control signals

D. Asserting Logic

The three outputs of detection logics are given with a certain amount of delay before they assert. The assert is shown in Fig.11. The delay Ǿ used to assert. Then output signals must be set in the range of ψ<Φ<δ. Where ψ - the delay in the data signal, δ - close-clock logic for the circuit of latch.

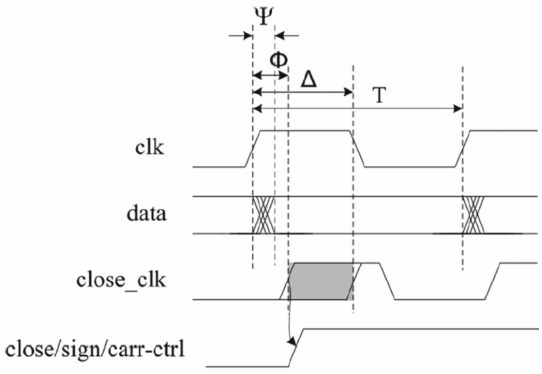

Fig. 11. Timing diagram of the control signals of detection logic circuits after assertions.

The range of ψ<Φ<δ is used to filter out the glitching signals as well as to keep the computation results correctly. Here ψ act as data transient period and δ denotes the earliest required time of all of the inputs. The range of ψ has been represented as shadow in the timing diagram. However the restriction that Φ must be greater than ψ to guarantee the registers from latching. The wrong values of control signals usually decrease the overall speed of the applied designs. The timing control of the delay Φ for the implementation of detection logic circuit using AND gate is slightly different from the first implementation using registers. That is the range of Φ can be set as θ<Φ<δ to filter out the glitch signals and to keep the computation results correct. This computation allows upper level systems to assert the 'close' signal with an arbitrary short delay closing to the positive edge of the clock signal, which provides a more flexible controlling space for the delay Ø. Thus the detection logic circuit and asserting logic will give better control over the low power multiplier.

IV. PERFORMANCE EVALUATION

The SPSIT-equipped multiplier design can be realized by the standard cell-based design flow with an in-house 0.18-mm CMOS cell library. This design is verified via C/MATLAB behavioural simulation, nLint HDL coding rule check, VHDL/Verilog RTL simulation, SYNOPSYS logic synthesis, VHDL/Verilog gate-level simulation, and NanoSim transistor-level simulation.

Table 2. Performance comparison

Design	Power / MHz (P.mw)	Maximum Frequency
Original tree MUI	0.0200	200MHz
SPSIT using Register	0.0118	142MHz
SPSIT using AND Gate	0.0121	210MHz

V. SIMULATION RESULTS

The following figures (Fig.12 and Fig.13) show the simulation results of the design with register and AND gate in the detection circuit.

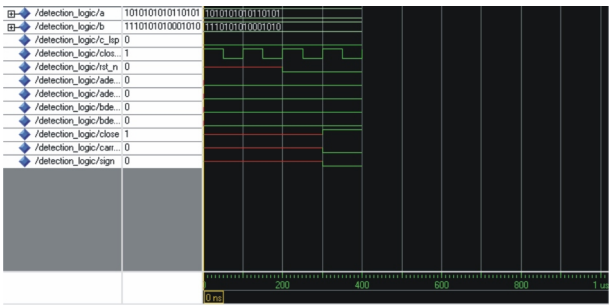

Fig.12. Detection Logic Circuit Design Using registers

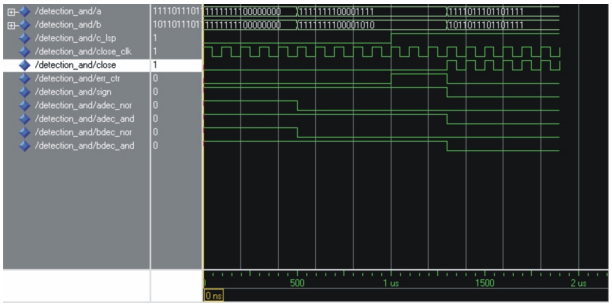

Fig.13. Detection Logic Circuit Design Using AND Gate

VI. CONCLUSION

In this paper, MAC unit adopting the SPSIT approach using register and AND gates in the detection logic unit is presented. The simulation results show that the power reduction of the new approach, which leads to a 40% switching power swiftness improvement when compared with the existing techniques in 0.18-mm CMOS technology. In addition, it can be seen that the performance can also be improved considering the design with different bit-width input data. The results also show that the SPSIT approach not only owns equivalent low-power performance but also leads to a higher maximum speed when compared with the other approaches. Moreover, the proposed SPSIT-equipped MAC also has better power efficiency when compared with the existing modern MAC unit.

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