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SIGMA DELTA MODULATOR FOR BIOMEDICAL APPLICATIONS WITH REDUCED NONIDEALITIES

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Abstract

A low power second order sigma-delta modulator (ΣΔM), for biomedical applications, has been presented in this paper. This can be used to digitize electrical biomedical signals like Electro-cardiogram (ECG), Electroencephalogram (EEG), and Electroretinogram (ERG). The proposed sigma delta modulator has been implemented by Switched Capacitor (SC) technique. Behavioral modeling of nonideal second order SC ΣΔM was done to find out the integrator's opamp specifications to attain resolution of 10 bits. Integrator has been designed to minimize distortion and charge injection, and remove input dependent offset voltage. Dynamic latched comparator has been employed for power reduction. The feedback circuit has been designed for minimum usage of switches and capacitors. The simulated results of the proposed ΣΔM in standard CMOS 0.18 µm technology, using Tanner tools gives > 10 bits resolution and power consumption ranges from 50 µW to 400 µW with a 1.8 V power supply.

Key words: Biomedical application, SD Toolbox, Second Order Sigma-delta modulator.

I. INTRODUCTION

In biomedical instrumentation, biomedical signals such as Electrocardiogram (ECG), Electroencephalogram (EEG), Electrogastrogram (EGG), Electroretinogram (ERG) are analog in nature. The voltage and frequency ranges of some common biomedical signals are shown in Fig. 1 [1]. These biomedical signals are low frequency signals.

There is a necessity for biomedical signals to be converted into the digital domain for further analysis and signal processing using either conventional digital computers or special purpose digital signal processors (DSPs). As sigma-delta ADC can achieve the highest resolution for relatively low signal bandwidths [2], it is ideally suited for biomedical applications. In order to relax the anti-alias filter requirement and to minimize the digital noise coupling on chip, oversampled sigma-delta converters are used.

In analog circuit design, the voltage or current mode methodologies can be used for signal processing. In the voltage (current) mode design, information is encoded by voltage (current) or its derivatives. The Switched Capacitor (SC) technique has been extensively used in the voltage mode design while Switched Current (SI) techniques in the current mode design. Due to its ability to realize accurate signal processing function we have used SC technique.

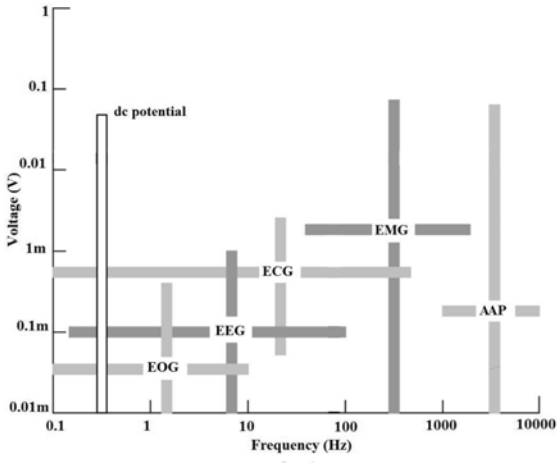

Fig.1 Voltages and Frequency Ranges of Some Common Bio-potential Signals [1]

In section II the behavioral modeling of ΣΔM has been presented. Section III discusses the circuit topologies for the design of low power low pass second order switched capacitor ΣΔM to achieve a resolution > 10 bits suitable to digitize biomedical signals such as ECG. Section IV presents the simulation results obtained.

II. SYSTEM LEVEL ARCHITECTURE

As the order of ΣΔM goes beyond two, the system experiences potential instability while the usage of first order modulator to achieve required dynamic range results in large over sampling ratio (OSR) thus large power. A multibit quantizer produces harmonic distortion due to step-size mismatch [3]. Thus, second order modulator with 1-bit quantizer is used in our design.

The architecture implementation of second order ΣΔM is shown in Fig. 2. The values for integrators' gain b_1 and b_2 are used to protect integrators from saturation. MATLAB Simulink has been widely accepted to model and simulate ΣΔM.

The output spectrum for the ideal modulator simulated using MATLAB and SIMULINK environment is shown in Fig. 3 for a sinusoidal input signal with 0.2 V amplitude and 200 Hz frequency.

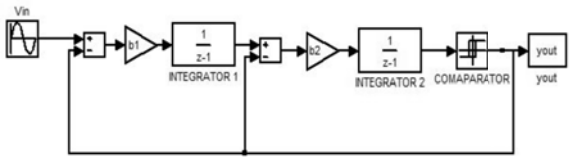

Fig.2 Ideal Second Order Sigma Delta Modulator

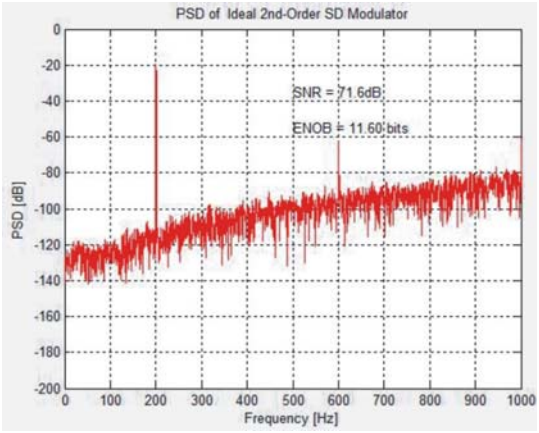

Fig. 3 PSD for Iideal Second Order ΣΔM

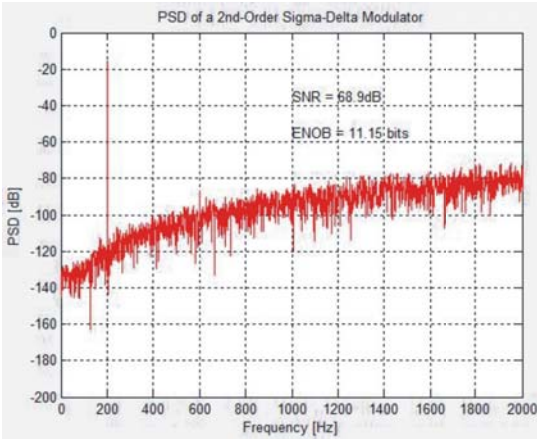

Fig. 4 PSD for Nonideal 2nd Order ΣΔM

But in real-time simulations, the modulator includes many non-idealities. The most important non-idealities such as sampling jitter, kT/C noise, internal ADC/DAC's parameters mismatch and non-linearity, operational amplifier parameters (white noise, 1/f noise, finite dc gain, finite bandwidth, slew rate and saturation voltages) have been modeled in Simulink, using SD toolbox. The SD toolbox is a toolbox created to simulate Switched Capacitor (SC) ΣΔM at behavioral level, within Simulink environment [4], [5].

And the behaviorally modeled nonideal second order modulator resulted in Power Spectral Density (PSD) as shown in Fig. 4. The Signal to Noise Ratio (SNR) for ideal modulator is 71.6 dB while the SNR for non-ideal modulator is 68.9 dB.

III. CIRCUIT LEVEL IMPLEMENTATION

A. Two Stage Opamp

Switched capacitor integrator consists of opamp, switches and capacitors. A high gain opamp should be used for integrator to work properly. Hence, to meet the requirements of a high gain input stage and an output stage with high driving capabilities, a two stage opamp is used. Miller compensation technique is employed for its stability in closed-loop applications. Due to an unintentional feed-forward path through the Miller capacitor, a Right-Half-Plane (RHP) zero is resistor is inserted in series with the Miller capacitor to remove this RHP zero [6].

The differential pair in Fig. 6 is formed by n-channel MOSFETs, M1 and M2. The first stage gives a high differential gain and performs the differential to single ended conversion. The first stage of op-amp has the current mirror circuit formed by p-channel MOSFETs M3 and M4. The transistor M6 serves as a n-channel common source amplifier which is the second stage of opamp and is aided by current load M7.The bias of the opamp circuit is provided by M8 and I_B [7], [8]. The opamp is designed to attain the specifications given in Table I.

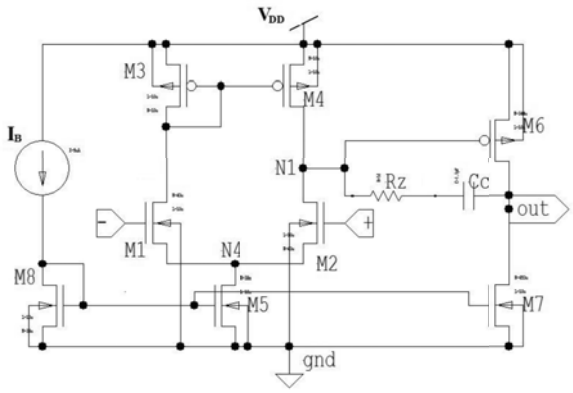

Fig. 5 Two Stage Opamp [7]

B. Parasitic Insensitive Switched Capacitor Integrator

The single ended SC integrator which is parasitic insensitive is shown in Fig. 6. It is driven by two non-overlapping clock phases P1 and P2. During the phase P1, integrator is in sampling mode and in phase P2, it is in integrating mode. The capacitors C1, C2 perform the integration, while C3 is an auxiliary capacitor used to compensate for the finite gain error and the offset voltage of the amplifier [9]. During phase 1, C1 is directly connected across the amplifier.

To minimize distortion, dc error and to keep dc offset low, clocks P_1, P_2, P_{1a} (slightly advanced wrt P1) are employed to turn off the switches near the virtual ground first.

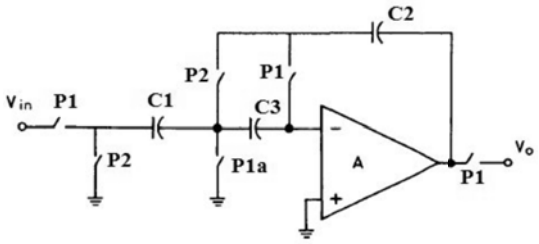

Fig. 6 Switched Capacitor Integrator [9]

By delaying clock P_1, for switch S1 wrt clock P_{1a} for switch S3, the input dependent offset voltage appearing at the output can be removed [7]. And switches connected to ground or virtual ground is realized using nmos switch to reduce the charge-injection effects [8].

C. Comparator

To reduce power, dynamic latch comparator is used which removes the need for pre-amplifying stage. [10] The 'Lewis-Gray' dynamic comparator shown in Fig. 7 was introduced by [11].

The operation of the comparator is as follows. When the clock signal is low, the transistors M9 and M12 are conducting and M7 and M8 are cutoff, which forces both differential outputs to V_{DD} and no current path exists between the supply voltages. Simultaneously M10 and M11 are cutoff and the transistors M5 and M6 conduct. This implies that M7 and M8 have have a voltage of V_{DD} over them. When the comparator is latched, the control signal goes up (clock=V_{DD}), which turns M7 and M8 on. Immediately after the switching moment, the gates of the transistors M5 and M6 are still at V_{DD} and they enter saturation. The imbalance of the conductances of the left and right input branches formed by M1, M2, M5 and M3, M4, M6 determines which of the outputs goes to V_{DD} and which to 0 V. After a static situation is reached when clock=V_{DD}, both branches are cutoff and the outputs preserve their values until the comparator is reseted again by switching latch to 0 V.

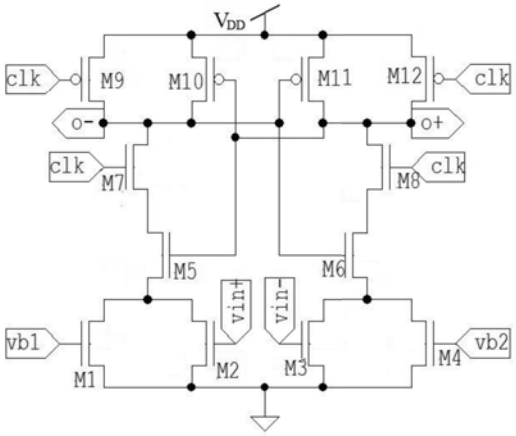

Fig. 7 Dynamic Comparator

The transistors connected to the input and reference M1-M4 are in the triode region and act like voltage controlled resistors. If no mismatch is present, the comparator changes its output when the conductances of the left and right input branches are equal. By denoting $W_A = W_1 = W_3$ and $W_B = W_2 = W_4$ the input voltages when the comparator changes the state is given by

$$V_{+in} - V_{-in} = \frac{W_B}{W_A}(V_{+ref} - V_{-ref}) \quad (1)$$

By dimensioning of the transistors width W_A and W_B, the threshold of the comparator can be adjusted to the desired level.

The comparator produces output of V_{DD} when it is in reset mode. But in order to hold the previous value during reset an SR latch is used after passing the differential outputs through inverter.

D. 1-bit DAC and Summer Implementation

The circuit implementation for feedback from comparator output to input of integrator through 1-bit DAC is achieved by implementing two input switched capacitor integrator, where one input is the input signal and second input is $-V_{ref}$ or $+V_{ref}$ depending on the output signal 'y' i.e. if y=0, $-V_{ref}$ is feedback and if y=1, V_{ref} [12] as shown in Fig. 8.

E. Complete Circuit Diagram of Second Order SDM

Fig. 9 shows the complete second order ΣΔM. The feedback is designed to reduce number of switches and capacitors. During clock phase P1 the first integrator will be in sampling mode. During the clock phase P2, the first integrator is in integrating mode and the second one is in

sampling mode. Now the comparator output is sensed at the beginning of the clock and latched. The output of comparator is used to provide feedback by applying $+V_{ref}$ to second input of integrators, if output y is high and $-V_{ref}$, if y is low. The feedback circuitry is designed to consume less area and power by reducing the number of switches and capacitors.

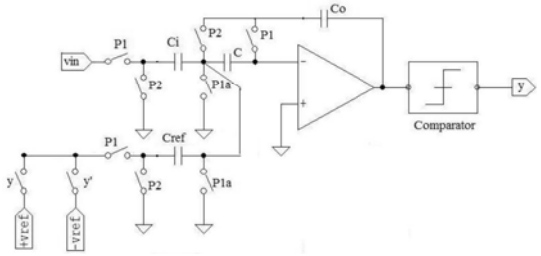

Fig. 8 First Order SD Modulator

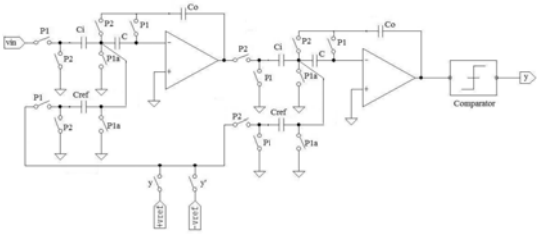

Fig. 9 Second Order SD Modulator

IV. RESULTS AND CONCLUSION

From the behavioral modeling of the modulator, integrators' gain coefficients (b1 and b2), and opamp specifications are obtained, to achieve SNR of about 70 dB for input signal frequency of 200 Hz and OSR 64.

TABLE I
SPECIFICATIONS OF OP AMP

Parameter	Simulated Result
DC Gain (A_{vo})	> 45 dB
Unity Gain Bandwidth (UGB)	15 MHz
Slew Rate (SR)	10 V/μs
Phase Margin (PM)	> 60 deg

n technology node using power supply voltage of 1.8V. Tanner tools are used to simulate the above designed circuit. The total power consumed by the proposed ΣΔM ranges from 50 μW to 400 μW.

Thus, a low power low pass ΣΔM has been designed with reduced nonidealities, so that dynamic range of >10 bits is met.

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