LOW-COMPLEXITY HIGH-SPEED QUASI-CYCLIC LDPC CODED MODULATION IN OFDM WIRELESS COMMUNICATION SYSTEM

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Abstract

This paper investigates a Low-Density Parity-Check (LDPC) coded rthogonal Frequency-Division Multiplexing (OFDM) wireless communication system based on IEEE 802.11a standard. This paper studies low-complexity high speed decoder architectures for quasi-cyclic low density parity check (QC-LDPC) codes. Algorithmic transformation and architectural level optimization are incorporated to reduce the critical path and bit error rate (BER). Enhanced partially parallel decoding architectures are proposed to linearly increase the throughput of conventional partially parallel decoders through introducing a small percentage of extra hardware. The LDPC decoding procedure is simplified without the estimation of channel noise power. Simulation results show that this algorithm is effective and the decoding performance is satisfied when maximum iteration number is 10.

Key words: IEEE 802.11a standard; LDPC coded; quasi-cyclic (QC) codes; Modulation; OFDM system; decoding initialization algorithm.

I. INTRODUCTION

Orthogonal Frequency Division Multiplexing (OFDM) is a very attractive technique for high-bitrate data transmission [1] in frequency selective channel because it can eliminate the Intersymbol interference (ISI). And this technique is applied in some Wireless Local Access Networks (WLAN) standards such as IEEE 802.11a in USA and HiperLAN/2 in Europe. On the other hand, Low-Density Parity-Check (LDPC) codes, first introduced by Gallager in 1962, have near Shannon limit performance when decoded using an iteratively probabilistic algorithm. In this paper, we studied the quasi-cyclic LDPC coded OFDM wireless communication system based on IEEE 802.11a standard. Simulation results show that this algorithm is effective and can make decoding rapidly.

II. LDPC CODED OFDM SYSTEM

Recently, a class of structured low density parity check (LDPC) codes, namely quasi-cyclic (QC) LDPC codes , that can achieve comparable performance to computer generated random codes has been proposed and shown in figure 1. QC-LDPC codes are well suited for hardware implementation. The encoder of a QC-LDPC code can be easily built with shift-registers while random codes usually entail complex encoding circuitry to perform complex matrix and vector multiplications. In addition, QC-LDPC codes also facilitate efficient high-speed decoding due to the regularity of their parity check matrices. On the other hand, randomly constructed LDPC codes require complex routing in the (hardware) decoders, which not only consumes a large amount of chip area, but also significantly increases the computation delay. For instance, a fully parallel decoder based on direct mapping presented in for a rate-1/2 1024-bit LDPC code consumed 1.7-M gates with a maximum (source data) decoding throughput of 500 Mb/s.

III. LDPC ARCHITECTURE

Low-density parity-code (LDPC) codes are a class of linear error-correcting codes. Linear codes use a generator matrix G to map message s to transmitted blocks t, also known as codeword. They have an equivalent description in terms of a related paritycheck matrix H. All codewords satisfy H·t=0.

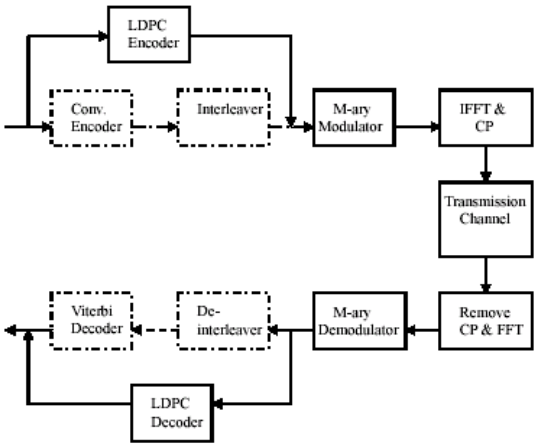

Fig. 1. Block diagram of LDPC based OFD system

$$\mathbf{H} = \begin{bmatrix} 1 & 0 & \cdots & 1 & \cdots & 0 & \cdots & 0 \\ 0 & 1 & \cdots & 1 & \cdots & 1 & \cdots & 0 \\ \vdots & \vdots & & \vdots & & \vdots & & \vdots \\ 1 & 0 & \cdots & h_{i,j} & \cdots & 0 & \cdots & 0 \\ \vdots & \vdots & & \vdots & & \vdots & & \vdots \\ 0 & 0 & \cdots & 0 & \cdots & 0 & \cdots & 1 \end{bmatrix}$$

Fig. 2. LDPC Architecture

The parity check matrix H for LDPC codes is a sparse binary matrix. The general structure of H is shown fig 2. Each row of H corresponds to a parity check and a set element *hi, j* indicates that data symbol *j* participates in parity check *i*. In a block of n bits or symbols, there are m redundant parity symbols and the code rate is r given by $r = (n - m)/n$. The set row and column elements of H are chosen to satisfy a desired row and column weight profile, where the row and column weights are defined as the number of set elements in a given row and column, respectively. In a *regular* LDPC code, all rows are of uniform weight, as are all columns. An *irregular* LDPC code is defined by a parity-check matrix H with multiple column weights and multiple row weights. Therefore, based on the *irregular* LDPC definition, the convolution code can be look as a kind of *irregular* LDPC, it apply that it could decode by the corresponding decoding algorithm. We will demonstrate the decoding performance with the 802.11a standard in the following section.

IV. PARTIALLY PARALLEL LDPC DECODING ARCHITECTURE

Several papers have addressed partially parallel decoding architectures for regular LDPC codes. These architectures generally achieve a good tradeoff between hardware complexity and decoding throughput. A partially parallel decoder architecture for generic (3, 5) QC-LDPC codes is shown in Fig 2, where totally memory banks are used to store the soft message symbols conveyed at both decoding phases, memory bank 's are used to store the intrinsic information and memory bank C's are used to store the decoded data bits. For QCLDPC codes, the address generator for each memory bank can be realized with a simple counter, which not only simplifies the hardware design, but also improves the circuit speed. In general, each node processing unit takes 1 clock cycle (assuming dualport memories are used, otherwise two cycles are needed) to complete message updating for one row (or column) of the parity check matrix. Fig 3, 4, 5 shows a small sub-matrix of a QC-LDPC parity check matrix, where all 1-components are numbered starting from the first row. With the conventional partially parallel decoding approaches, 14 memory entries need to be allocated for the corresponding memory bank. All the soft messages corresponding to 14 1-components shown in Fig are stored sequentially in the memory. In the row decoding phase (i.e., the check-to-variable message passing phase), the memory address generator generates 0, 1, 13. In the column decoding phase (i.e., the variable-to-check message passing phase), the address generator outputs 9, 10, 13, 0, 1, 8. Hence, the address generator can be implemented as a simple modulo-13 counter.

It should be mentioned that such a high decoding throughput can be attributed to two factors: 1) Very high clock speed resulted from various architectural level and circuit level optimizations and 2) Enhanced parallelism in partly parallel decoding.

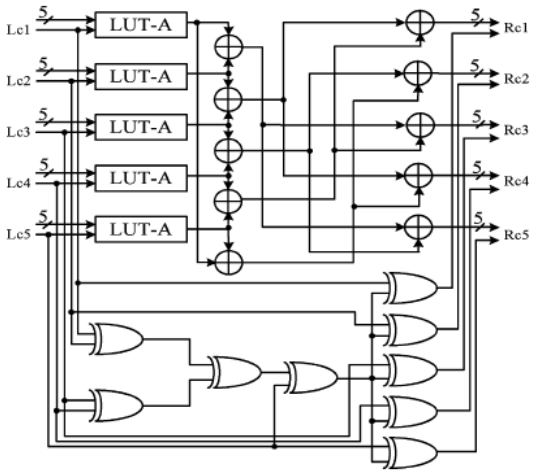

Fig. 3. Optimized architecture for CPU

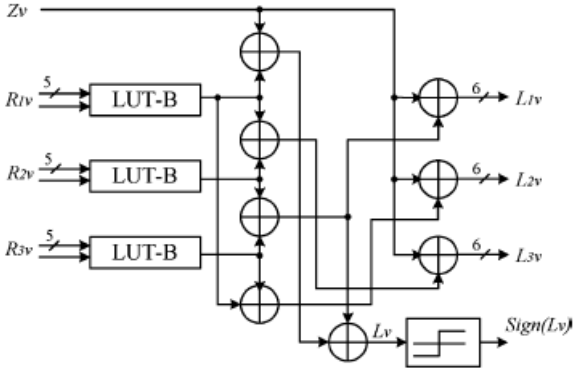

Fig. 4. Optimized architecture for VPU

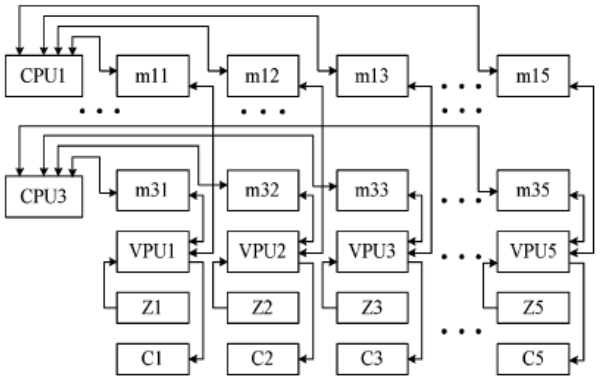

Fig. 5. Structure of a partially parallel decoder for (3, 5) QC-LDPC codes

V. SYSTEM DESIGN AND SIMULATION RESULTS

Based on the architectures, partially parallel LDPC based OFDM was modeled in VHDL and simulated using ModelSim. We then synthesized and performed place and route for the design using the Xilinx ISE 9.1i software package. The platform has special part in the receiver that it is used the LDPC-Based decoder to substitute for conventual's Viterbi decoder. In this study, our proposed method only uses the AWGN as a channel condition; hence, it is unnecessary to design the equalizer for channel estimation in the simulation processing Fig 7. From our simulation result, one fact is found that the LDPC-Based decoder can only be used to error correction of codeword of Convolutionnal code. The messages ˆs still utilizes the linear block decoding algorithm. In this study, we demonstrated a decoding method, in the case of a binary symmetric channel, as following. In the LDPC-Based decoding procedure, we have to choose a suitable size of generator matrix G via transmission signal frame length and the code rate. Because the generator matrix G is a rectangular matrix, an inverse G- 1 of the matrix in modulo 2 arithmetic has been computed during the Gaussian elimination which produced the matrix R = G*T* (G · G*T*)-1 such that G · R = G · G*T* (G · G*T*)-1 = I. According to the linear block code encoder s·G=t, the messages ˆs in the receiver could estimate by ˆs=t·R. Consequently, the original messages can be easily estimated.

The simulation performance of the proposed LDPCBased decoding algorithm is shown in table 1. They include comparisons of different modulation, including 16-QAM and QPSK, and demonstrate the realistic performances of ofdm systems with LDPC Based decoder under AWGN and Rayleigh fading channels, respectively.

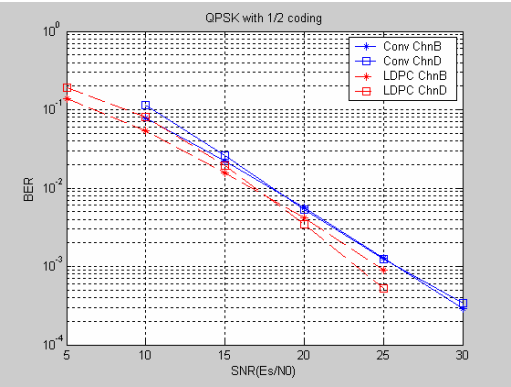

Fig. 6.1a BER performance comparison of regular LDPC and CC with QPSK, ˝ and QAM coding.

In Fig, the user moving with the velocity 30km/hr, central frequency 2.5GHz, and subcarrier bandwidth 3.5MHz. From the simulation results, it can be found that the proposed method still possesses a high error correction capability under different noise interferences. Apparently, from the indications of the above simulation results, the proposed method can substitute for Viterbi decoder with its simple structure although it sacrifices some performance. Based on this design procedure, it is no doubt that the SOC design for ofdm system in the future can effectively utilize one decoder for decoding two kinds of encoder. Therefore, the proposed method is very suitable for practical applications in the ofdm communication systems.

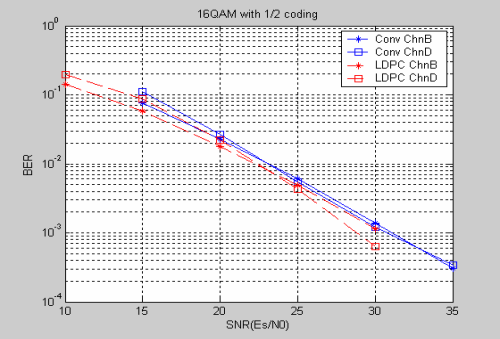

Fig. 6.1b BER performance comparison of regular LDPC and CC with QPSK, ˝ and QAM coding

Table 1 Comparison of FFT Algorithm based on Block multipliers and CLB Slices.

FFT Algorithm	Block Multipliers	CLB Slicers
Radix 2	32	384
Radix 4	16	392
Split Radix	12	288

The BER performance versus Signal-Noise-Ratio (SNR) of different data rate is shown in (solid curves). In general, when the data rate or the spectral efficiency increases the power loss increases.. In addition, we observe that the scheme of 12Mbits/s with code rate ˝ and QPSK modulation outperforms Fig 6.1a and 1b. Here the influence to performance by the code rate is larger than that of by the modulation. For instance, when BER is 10^{-5}, 12Mbits/s scheme has a power gain of 2dB. For analysis purpose, the point FFT is chosen and the comparison table shows the number of CLB slices and block multipliers for different FFT architectures Table 1 and synthesize result shown in Table 2.

Table 2 Synthesize result

Device Utilization for 2V40cs144 of LDPC

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Resource	Used	Avail	Utilization
IOs	43	88	48.86%
Function Generators	139	512	27.15%
CLB Slices	70	256	27.34%
Dffs or Latches	40	776	5.15%

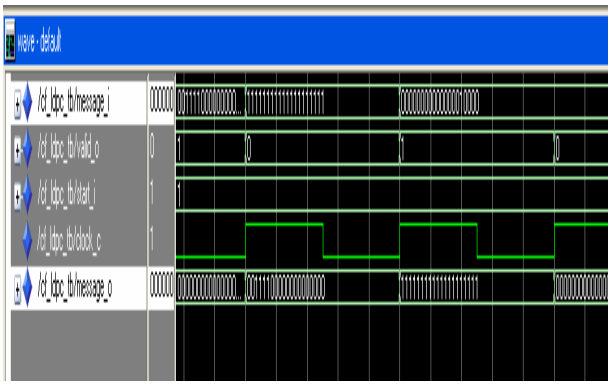

Fig .7 Simulation result

VI. CONCLUSION.

In this paper, we evaluated the performance of the LDPC based OFDM systems. We showed that the LDPC-OFDM systems achieve the good error rate performance with a small number of iterations on both an AWGN and a frequency-selective fading channel. We also showed architectural optimizations to reduce the clock period for LDPC decoders and developed enhanced partially parallel decoder architectures to linearly increase the decoding throughput with a small amount of extra hardware.

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