PINCH RESISTOR ANALYTICAL MODELING WITH SIMPLE MODEL
AND JFET MODEL FOR VLSI DESIGN

Pushpinder Singh¹, Balwant Raj², Balwinder Raj³
¹²³University Centre for Instrumentation and Microelectronics (UCIM)
Panjab University Chandigarh, Chandigarh (India)
²Sant Baba Bhag Singh Institute of Engineering and Technology, Jalandhar (India)
E-mail: balwinderraj@gmail.com

Abstract

Analytical modeling of pinch resistor has been carried out in this paper using the simple model and JFET model. The results obtained through the simple model are compared with the JFET model, which shows that the JFET model is more robust for the VLSI design. The analysis and design of ICs depend heavily on the utilization of suitable models for IC components. A device technologist designs for circuits applications while process technologist develops process to fabricate these devices. For the same channel width and doping concentration for \( N = 5 \times 10^{17}/cm^2 \), the resistance of the pinch resistor 1.44 times greater than the N-well device resistor, and for the doping concentration \( N = 5 \times 10^{11}/cm^2 \), the resistance of the pinch resistor 1.35 times greater than the N-well device resistor.

Keywords: Wind Farm, Induction Generator, Point of Common Coupling (PCC), Voltage Source Converter (VSC), Flexible AC Transmission Systems (FACTS), Pulse Width Modulated (PWM) inverter.

I. INTRODUCTION

The fundamental goal in device modeling is to obtain fundamental relationship among the electrical variables of the device that is to be modeled. The electrical characteristics depend upon a set of parameters including both the geometrical variables and variables depend on the device physics. The sheet resistance can be increased of the N-well resistor by diffusing a P⁺ layer, which is made floating. The P⁺ layer reduces the cross-section available to current flow. The P⁺ layer also shields the resistor from above, thus eliminating the capacitive coupling between the resistor and any interconnection lines that might be passing above it. This resistor is called the pinch resistor because the conducting area is decreased for the current, and high values of sheet resistances is obtained, comparative to the N-well. Typically the models are initially developed by analytically applying basic physical principles and then empirically modifying the resulting mathematical expressions to improve agreements between theoretical and experimental results. The N-well resistor can be modeled in two ways:

1. Simple model of pinch resistor.
2. JFET model of pinch resistor.

II. SIMPLE MODE OF PINCH RESISTOR

In this model we assume the voltages at two terminals (n⁺) are same with respect to the substrate and doping concentration is same thought the N-well. The figure shows the schematic of the N-well device resistor used for modeling. There is a pn junction between the substrate and N-well that is reversed biased in normal operation. The P⁺ region made floating for the normal operation. The device resistance is mainly determined by the resistivity and the geometry is given as-

\[ 0 \int_y d^y L; \]
\[ 0 \int_z d^z W; \]
\[ 0 \int_x d^x xj; \]

Where \( x_j \) is the depth of the N-well to substrate metallurgical junction and \( L \) is the length of the channel and \( W \) is the width of the channel. A depletion region exists.
at the bottom side and ends of sidewall the N-well region. The depletion region thickness and thus resistance of the device is modeled by junction bias.

By taking an assumption that we are applying a same voltage on both n+ terminals, the resulting thickness of the depletion region will be constant through out the junction. Let the substrate terminal is at ground potential. Since we are taking only n side depletion region in account.

The depletion layer between the p-substrate and n-well region is given as:

\[ X_{d1} = \left( \frac{2 \varepsilon_S N_{d1}}{qN_d (N_a + N_d)} \right)^{1/2} (V + V_{b1})^{1/2} \]

(1)

The depletion layer between the p+ cap and n-well region is given as:

\[ X_{d2} = \left( \frac{2 \varepsilon_S N_{d2}}{qN_d (N_a + N_d)} \right)^{1/2} (V_{b2})^{1/2} \]

(2)

Built in potential between the p-substrate and n-well region

\[ V_{b1} = \frac{KT}{q} \ln \left( \frac{N_{d1} N_d}{n_i^2} \right) \]

(3)

Built in potential between the p+ cap and n-well region

\[ V_{b2} = \frac{KT}{q} \ln \left( \frac{N_{d2} N_d}{n_i^2} \right) \]

(4)

The resistivity of the N-well is given by

\[ \rho = \frac{1}{qN_j \mu} \]

The dependence of mobility on doping concentration is given as

\[ \mu = \mu_{\text{min}} + \frac{\mu_{\text{max}} - \mu_{\text{min}}}{1 + \left( \frac{N}{N_{\text{ref}}} \right)^{N_p}} \]

(5)

Now sheet resistance is given as

\[ R_{sh} = \frac{\rho}{X_n} \]

Where

\[ X_n = X_j - X_{j1} - X_{d1} - X_{d2} \]

And the total resistance will be

\[ R = \frac{R_{sh} L}{W_{eff}} = \frac{\rho L}{(X_j - X_{j1} - X_{d1} - X_{d2}) (W - 2X_{d1})} \]

(6)

Fig. 2. Cross section along channel of Pinch Resistor for Advance (JFET) model.

III. JFET MODEL OF PINCH RESISTOR

The schematic diagram used for modeling of pinch resistor as a JFET model is shown in figure (2). In practical circuit, there is a voltage difference across the resistor terminals V1 and V2. Therefore the depletion width will linearly increase from terminal V1 to terminal V2 and resistor can be modeled as a JFET. The device geometry is same as in simple model.

The depletion region thickness and thus resistance of the device is modeled by the junction bias. Let at a position \( y \) along the length of the N-well resistor, an infinitesimally small slice with thickness \( dy \) has a voltage drop \( dV \). The width and the depth of the conducting (undepleted) portion of the resistor at this point in the channel are functions of the local resistor body bias with respect to the substrate.

Assuming an abrupt junction, the channel depth at point \( y \) is given by

\[ X_n(y) = X_j - X_{j1} - X_{d1} - X_{d2} \]

(7)

Where depletion width in N-well region is given as

\[ X_{d1} = \left( \frac{2 \varepsilon_S N_{d1}}{qN_d (N_a + N_d)} \right)^{1/2} (V_{y} + V_{b1})^{1/2} \]

(8)
\[
A_1 = \frac{2e \varepsilon n_{a1}}{q(N_{a1} + N_d)N_d}
\]

The depletion layer between the p' cap and n-well

\[
X_{d2} = \left(\frac{2e \varepsilon n_{a2}}{qN_d(N_{a2} + N_d)} \right)^{1/2} (V_{b2})^{1/2}
\]

\[
A_2 = \frac{2e \varepsilon n_{a2}}{qN_dN_{a2} + N_d}
\]

Where

- \(V_y\) is the resistor body (N-well) to substrate bias at \(y\).
- \(N_{a1}\) is the doping concentration of substrate.
- \(N_{a2}\) is the doping concentration of p' region.
- \(N_d\) is the doping concentration of N-well.

Built in potential between the p-substrate and n-well region

\[
V_{d1} = \frac{KT}{q} \ln \left( \frac{N_{a1} + N_d}{n^+} \right)
\]

Built in potential between the p' cap and n-well region

\[
V_{d2} = \frac{KT}{q} \ln \left( \frac{N_{a2} + N_d}{n^+} \right)
\]

The equation of the current density through the slice is given as

\[
J = qn v_d
\]

Where \(v_d\) is the drift velocity of the carrier.

\[
J = qn \mu E
\]

\[
J = qn \mu \frac{dV}{dy}
\]

Thus, the current through the infinitesimally small slice with dy length has a potential dV is given by multiplying cross sectional area with current density.

\[
I_d = qN_d \mu (X_y V_{b1}) \frac{dV}{dy}
\]

\[
I_d = qN_d \mu (X_y - X_{a1} - X_{d1} - X_{d2}) (W_{a1} - 2X_{d1}) \frac{dV}{dy}
\]

\[
I_d = qN_d \mu (X_y - X_{a1} - X_{d1} - X_{d2}) (W_{a1} - 2X_{d1}) \frac{dV}{dy}
\]

Let \(C_1 = qN_d \mu\)

\[
C_2 = X_y - X_{a1} - A_2 (V_{b2})^{1/2}
\]

\[
I_d = C_1 \left( C_2 - A_2 V_{b1} \right)^{1/2} (W - 2A_1(V_y + V_{b1})) \frac{dV}{dy}
\]

\[
I_d = C_1 \left( C_2 - A_2 V_{b1} \right)^{1/2} (W - 2A_1(V_y + V_{b1})^2 + 2A_2(V_y + V_{b1}) \frac{dV}{dy}
\]

Integrating above equation with limit 0 to \(y\) and 0 to \(d^+ V_d\) we will get total current flowing through the N-well and given as

\[
I_d = C_1 \left( C_2 V_y - (W + 2C_1(V_y + V_{b1})^2) \right) A_2 (V_y + V_{b1}) \frac{dV}{dy}
\]

Taking limits

\[
I_d = C_1 \left( C_2 V_y - \frac{2}{3} (W + 2C_1(V_y + V_{b1})^3) \right) A_2 (V_y + V_{b1}) \frac{dV}{dy}
\]

\[
I_d = C_1 \left( C_2 V_y - \frac{2}{3} (W + 2C_1(V_y + V_{b1})^3) \right) A_2 (V_y + V_{b1}) \frac{dV}{dy}
\]

Therefore, the resistance of the pinch resistor will be

\[
R = \frac{V}{I_d}
\]

IV. PINCH RESISTOR

Resistances at different voltages with different \(w\)

(a) At \(N_d=5 \times 10^{16} \text{ cm}^{-3}\) & \(X_{y}=1 \mu \text{m}\)

Table 1. For simple model

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>(W=2.5 \mu \text{m}) R (10^6)</th>
<th>(W=5 \mu \text{m}) R (10^6)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2.3051</td>
<td>1.1955</td>
</tr>
<tr>
<td>2</td>
<td>2.5174</td>
<td>1.5544</td>
</tr>
<tr>
<td>3</td>
<td>2.6268</td>
<td>1.1848</td>
</tr>
<tr>
<td>4</td>
<td>2.7288</td>
<td>1.2123</td>
</tr>
<tr>
<td>5</td>
<td>2.8261</td>
<td>1.2378</td>
</tr>
</tbody>
</table>

Table 2. For JFET model

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>(W=2.5 \mu \text{m}) R (10^9)</th>
<th>(W=5 \mu \text{m}) R (10^9)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2.2916</td>
<td>1.0992</td>
</tr>
<tr>
<td>2</td>
<td>2.3756</td>
<td>1.1147</td>
</tr>
<tr>
<td>3</td>
<td>2.4407</td>
<td>1.1331</td>
</tr>
<tr>
<td>4</td>
<td>2.4982</td>
<td>1.1409</td>
</tr>
<tr>
<td>5</td>
<td>2.5514</td>
<td>1.1641</td>
</tr>
</tbody>
</table>
(b) At \( N_d = 5 \times 10^{17} \text{ cm}^{-3} \) & \( X_{j1} = 1 \mu m \)

### Table 3. For simple model

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>( W = 2.5 \mu m )</th>
<th>( W = 5 \mu m )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.45822</td>
<td>0.22717</td>
</tr>
<tr>
<td>2</td>
<td>0.46092</td>
<td>0.22803</td>
</tr>
<tr>
<td>3</td>
<td>0.46320</td>
<td>0.22896</td>
</tr>
<tr>
<td>4</td>
<td>0.46521</td>
<td>0.22940</td>
</tr>
<tr>
<td>5</td>
<td>0.46703</td>
<td>0.22997</td>
</tr>
</tbody>
</table>

### Table 4. For JFET model

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>( W = 2.5 \mu m )</th>
<th>( W = 5 \mu m )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.45643</td>
<td>0.22661</td>
</tr>
<tr>
<td>2</td>
<td>0.45803</td>
<td>0.22711</td>
</tr>
<tr>
<td>3</td>
<td>0.45938</td>
<td>0.22754</td>
</tr>
<tr>
<td>4</td>
<td>0.46059</td>
<td>0.22793</td>
</tr>
<tr>
<td>5</td>
<td>0.46170</td>
<td>0.22828</td>
</tr>
</tbody>
</table>

(c) At \( N_d = 5 \times 10^{16} \text{ cm}^{-3} \) & \( X_{j1} = 3 \mu m \)

### Table 5. For simple model

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>( W = 2.5 \mu m )</th>
<th>( W = 5 \mu m )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.9345</td>
<td>4.3720</td>
</tr>
<tr>
<td>2</td>
<td>1.0262</td>
<td>4.7059</td>
</tr>
<tr>
<td>3</td>
<td>1.1123</td>
<td>5.0168</td>
</tr>
<tr>
<td>4</td>
<td>1.1970</td>
<td>5.3177</td>
</tr>
<tr>
<td>5</td>
<td>1.2820</td>
<td>5.6152</td>
</tr>
</tbody>
</table>

### Table 6. For JFET model

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>( W = 2.5 \mu m )</th>
<th>( W = 5 \mu m )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.8409</td>
<td>4.0914</td>
</tr>
<tr>
<td>2</td>
<td>0.9171</td>
<td>4.3118</td>
</tr>
<tr>
<td>3</td>
<td>0.9629</td>
<td>4.4908</td>
</tr>
<tr>
<td>4</td>
<td>1.0082</td>
<td>4.6300</td>
</tr>
<tr>
<td>5</td>
<td>1.0504</td>
<td>4.7096</td>
</tr>
</tbody>
</table>

(d) At \( N_d = 5 \times 10^{17} \text{ cm}^{-3} \) & \( X_{j1} = 1 \mu m \)

### Table 7. For simple model

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>( W = 2.5 \mu m )</th>
<th>( W = 5 \mu m )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4.5822</td>
<td>2.2717</td>
</tr>
<tr>
<td>2</td>
<td>4.6092</td>
<td>2.2803</td>
</tr>
<tr>
<td>3</td>
<td>4.6230</td>
<td>2.2876</td>
</tr>
<tr>
<td>4</td>
<td>4.6251</td>
<td>2.2940</td>
</tr>
<tr>
<td>5</td>
<td>4.6703</td>
<td>2.2997</td>
</tr>
</tbody>
</table>

(e) At \( N_d = 5 \times 10^{17} \text{ cm}^{-3} \) & \( X_{j1} = 3 \mu m \)

### Table 8. For JFET model

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>( W = 2.5 \mu m )</th>
<th>( W = 5 \mu m )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.4462</td>
<td>7.2338</td>
</tr>
<tr>
<td>2</td>
<td>1.4603</td>
<td>7.2544</td>
</tr>
<tr>
<td>3</td>
<td>1.4721</td>
<td>7.2703</td>
</tr>
<tr>
<td>4</td>
<td>1.4826</td>
<td>7.3109</td>
</tr>
<tr>
<td>5</td>
<td>1.4922</td>
<td>7.3477</td>
</tr>
</tbody>
</table>

### Table 9. For simple model

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>( W = 2.5 \mu m )</th>
<th>( W = 5 \mu m )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.4365</td>
<td>7.1338</td>
</tr>
<tr>
<td>2</td>
<td>1.4451</td>
<td>7.1661</td>
</tr>
<tr>
<td>3</td>
<td>1.4522</td>
<td>7.1933</td>
</tr>
<tr>
<td>4</td>
<td>1.4585</td>
<td>7.2177</td>
</tr>
<tr>
<td>5</td>
<td>1.4642</td>
<td>7.2399</td>
</tr>
</tbody>
</table>

---

**Fig. 8.** Pinch resistor for simple model: \( N_d = 5 \times 10^{16} \text{ cm}^{-3} \), \( W = 2.5 \mu m \), \( X_{j1} = 3 \mu m \).

**Fig. 9.** Pinch resistor for simple model: \( N_d = 5 \times 10^{17} \text{ cm}^{-3} \), \( W = 2.5 \mu m \), \( X_{j1} = 1 \mu m \).
Fig. of pinch resistor for simple model:
\[ N_d = 5 \times 10^{16} / \text{cm}^3, W=5\mu m, X_{j1}=3\mu m \]

Fig. of pinch resistor for JFET model for:
\[ N_d = 5 \times 10^{16} / \text{cm}^3, W=2.5\mu m, X_{j1}=1\mu m \]

Fig. of pinch resistor for simple model:
\[ N_d = 5 \times 10^{17} / \text{cm}^3, W=2.5\mu m, X_{j1}=1\mu m \]

Fig. of pinch resistor for JFET model for:
\[ N_d = 5 \times 10^{17} / \text{cm}^3, W=5\mu m, X_{j1}=3\mu m \]

Fig. of pinch resistor for simple model:
\[ N_d = 5 \times 10^{17} / \text{cm}^3, W=2.5\mu m, X_{j1}=3\mu m \]

Fig. of pinch resistor for JFET model for:
\[ N_d = 5 \times 10^{17} / \text{cm}^3, W=2.5\mu m, X_{j1}=3\mu m \]
V. CONCLUSION

In this paper analytical modeling of pinch resistor has been carried out using the simple model and JFET model. The results obtained through the simple model are compared with the JFET model, which shows that the JFET model is more robust for the VLSI design. For the same channel width and doping concentration for \( N_d = 5 \times 10^{15} \text{cm}^{-3} \), the resistance of the pinch resistor (for depth of the layer \( P \), \( X_j = 3 \text{um} \)) 6 times greater than the N-well device resistor, and for the doping concentration \( N_d = 5 \times 10^{17} \text{cm}^{-3} \), the resistance of the pinch resistor (for depth of the layer \( P \), \( X_j = 3 \text{um} \)) 4.2 times greater than the N-well device resistor.

REFERENCES


