PINCH RESISTOR ANALYTICAL MODELING WITH SIMPLE MODEL AND JFET MODEL FOR VLSI DESIGN

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Abstract

Analytical modeling of pinch resistor has been carried out in this paper using the simple model and JFET model. The results obtained through the simple model are compared with the JFET model, which shows that the JFET model is more roburst for the VLSI design. The analysis and design of ICs depend heavily on the utilization of suitable models for IC components. A device technologist designs for circuits applications while process technologist develops process to fabricate these devices. For the same channel width and doping concentration for N_d= 5x10^{16}/cm^3, the resistance of the pinch resistor 1.44 times greater than the N-welll device resistor, and for the doping concentration N_d=5*10^{17}/cm^3,the resistance of the pinch resistor 1.35 times greater than the N-well device resistor.

Keywords: Wind Farm, Induction Generator, Point of Common Coupling (PCC), Voltage Source Converter (VSC), Flexible AC Transmission Systems (FACTS), Pulse Width Modulated (PWM) inverter.

I. INTRODUCTION

The fundamental goal in device modeling is to obtain fundamental relationship among the electrical variables of the device that is to be modeled. The electrical characteristics depend upon a set of parameters including both the geometrical variables and variables depend on the device physics. The sheet resistance can be increased of the N-well resistor by diffusing a P^+ layer ,which is made floating. The P^+ layer reduces the cross-section available to current flow. The P^+ layer also shields the resistor from above, thus eliminating the capacitive coupling between the resistor and any interconnection lines that might be passing above it. This resistor is called the pinch resistor because the conducting area is decreased for the current ,and high values of sheet resistances is obtained, comparative to the N-well. Typically the models are initially developed by analytically applying basic physical principles and then empirically modifying the resulting mathematical expressions to improve agreements between theoretical and experimental results. The N-well resistor can be modeled in two ways:

1. Simple model of pinch resistor.
2. JFET model of pinch resistor.

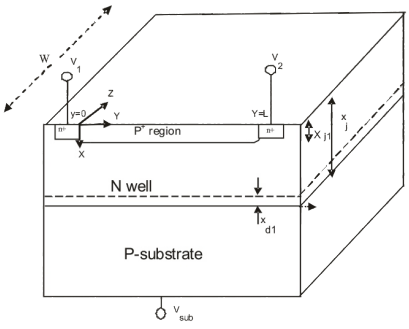


Fig. 1. Cross section along channel of Pinch resistor for simple model

II. SIMPLE MODE OF PINCH RESISTOR

In this model we assume the voltages at two terminals(n^+) are same with respect to the substrate and doping concentration is same thought the N-well. The figure shows the schematic of the N-well device resistor used for modeling. There is a pn junction between the substrate and N-well that is reversed biased in normol operation. The P^+ region made floating for the normal operation. The device resistance is mainly determined by the resistivity and the geometry is given as-

0 d" y d" L;

0 d" z d" W;

0 d" x d" xj;

Where x_j is the depth of the N-well to substrate metallurgical junction and L is the length of the channel and W is the width of the channel. A depletion region exists

at the bottom side and ends of sidewall the N-well region. The depletion region thickness and thus resistance of the device is modeled by junction bias.

By taking an assumption that we are applying a same voltage on both n^+ terminals, the resulting thickness of the depletion region will be constant through out the junction. Let the substrate terminal is at ground potential. Since we are taking only n side depletion region in account.

The depletion layer between the p-substrate and n-well region is given as:

$$X_{d1} \quad \frac{2 \ _{Si} N_{a1}}{qN_d \ N_a \quad N_d}^{1/2} \ V \quad V_{bi1}^{\ 1/2} \tag{1}$$

The depletion layer between the p^+ cap and n-well region is given as:

$$X_{d2} \quad \frac{2 \ _{Si} N_{a2}}{qN_d \ N_a \quad N_d}^{1/2} \ V_{bi2}^{\ 1/2} \tag{2}$$

Built in potential between the p-substrate and n-well region

$$V_{bi1} \quad \frac{KT}{q} \ln \ \frac{N_{a1} N_d}{n_i^2} \tag{3}$$

Built in potential between the p^+ cap and n-well region

$$V_{bi2} \quad \frac{KT}{q} \ln \ \frac{N_{a2} N_d}{n_i^2} \tag{4}$$

The resistivity of the N-well is given by

$$p \quad \frac{1}{qN_d}$$

The dependence of mobility on doping concentration is given as

$$_{min} \quad \frac{_{max} \quad _{min}}{1 \quad \frac{N}{N_{ref}}} \tag{5}$$

Now sheet resistance is given as

$$R_{sh} \quad \frac{p}{X_n}$$

Where

$$X_n \quad X_j \quad X_{j1} \quad X_{d1} \quad X_{d2}$$

And the total resistance will be

$$R \quad \frac{R_{sh.} L}{W_{eff}}$$

$$\frac{pL}{X_j \quad X_{j1} \quad X_{d1} \quad X_{d2} \ W \quad 2X_{d1}} \tag{6}$$

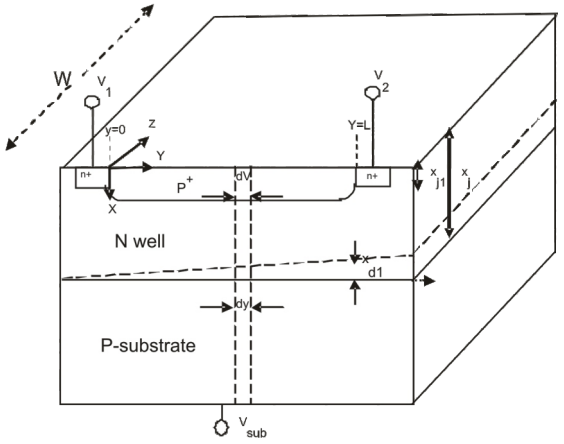


Fig. 2. Cross section along channel of Pinch Resistor for Advance (JFET) model.

III. JFET MODEL OF PINCH RESISTOR

The schematic diagram used for modeling of pinch resistor as a JFET model is shown in figure (2). In practical circuit, there is a voltage difference across the resistor terminals V_1 and V_2. Therefore the depletion width will linearly increase from terminal V_1 to terminal V_2 and resistor can be modeled as a JFET. The device geometry is same as in simple model.

The depletion region thickness and thus resistance of the device is modeled by the junction bias. Let at a position y along the length of the N-well resistor, an infinitesimally small slice with thickness dy has a voltage drop dV. The width and the depth of the conducting (undepleted) portion of the resistor at this point in the channel are functions of the local resistor body bias with respect to the substrate.

Assuming an abrupt junction, the channel depth at point y is given by

$$X_n(y) \quad X_j \quad X_{j1} \quad X_{d1} \quad X_{d2} \tag{7}$$

Where depletion width in N-well region is given as

The depletion layer between the p-substrate and n-well region

$$X_{d1} \quad \frac{2 \ _{Si} N_{a1}}{qN_d \ N_a \quad N_d}^{1/2} \ V_y \quad V_{b1}^{\ 1/2}$$

$$A_1 \ V_y \quad V_{b1}^{\ 1/2} \tag{8}$$

Where $A_1 = \dfrac{2\varepsilon_s N_{a1}}{q\left(N_{a1}+N_d\right)N_d}$

The depletion layer between the p^+ cap and n-well

$$X_{d2} = \left(\frac{2\varepsilon_{Si}N_{a2}}{qN_d\left(N_a+N_d\right)}\right)^{1/2}\left(V_{bi2}\right)^{1/2} \qquad (9)$$

$$= A_2\left(V_{b2}\right)^{1/2}$$

$$A_2 = \frac{\left(2\varepsilon_{si}N_{a2}\right)}{q\left(N_{a2}+N_d\right)}$$

Where V_Y is resistor body (N-well) to substrate bias at y.

N_{a1} is doping concentration of substrate

N_{a2} is doping concentration of p^+ region.

N_d is doping concentration of N-well.

Built in potential between the p-substrate and n-well region

$$V_{bi1} = \frac{KT}{q}\ln\left(\frac{N_{a1}N_d}{n_i^2}\right)$$

Built in potential between the p^+ cap and n-well region

$$V_{bi2} = \frac{KT}{q}\ln\left(\frac{N_{a2}N_d}{n_i^2}\right)$$

The equation of the current density through the slice is given as

$$J = qnv_d$$

Where v_d is the drift velocity of the carrier.

$$J = qn\mu E$$

$$J = qn\mu\frac{dV}{dy}$$

Thus, the current through the infinitesimally small slice with dy length has a potential dV is given by multiplying cross sectional area with current density.

$$I_d = qN_d\mu\left(X_n\right)\left(W_{eff}\right)\left(\frac{dV}{dy}\right)$$

$$I_d = qN_d\mu\left(X_j - X_{j1} - X_{d1} - X_{d2}\right)\left(W_{eff} - 2X_{d1}\right)\left(\frac{dV}{dy}\right)$$

$$I_d = qN_d\mu\left[\left(X_j - X_{j1} - A_2.\left(V_{b2}\right)^{1/2} - A_1\left(V_y+V_{b1}\right)^{1/2}\right)\left(W - 2.A_1.\left(V_y+V_{b1}\right)^{1/2}\right)\right]$$

Let $C_1 = qN_d\mu$

$$C_2 = X_j - X_{j1} - A_2.\left(V_{b2}\right)^{1/2}$$

$$I_d = C_1\left[\left(C_2 - A_2.V_{b1}\right)^{1/2}\left(W - 2.A_1.\left(V_y+V_{b1}\right)^{1/2}\right)\right]\frac{dY}{dv}$$

$$I_d = \left[C_1C_2W - C_1.A_1\left(V_y+V_{b1}\right)^{2}.W - C_1.C_2.2A_1\left(V_y+V_{b1}\right)^{2} + C_1.2.A_1^2\left(V_y+V_{b1}\right)\right]\frac{dV}{dy}$$

$$I_d\,dy = C_1\left[C_2W - \left(W + 2.C_2\right)\left(V_y+V_{b1}\right)^{2}.A_1 + 2.A_1^2.\left(Vy+V_{b1}\right)\right]dV$$

Integrating above equation with limit 0 d" y d" L and 0 d" V d" Vd, we will get total current flowing through the N-well and given as

$$I_d = C_1\left[C_2W.V_d - \left(W + 2.C_2\right)\left(V_y+V_{b1}\right)^{3/2}.A_1.\frac{2}{3} + A_1^2.\left(Vy+V_{b1}\right)\right]$$

Taking Limits

$$I_d = \frac{C_1}{L}\left[C_2W.V_d - \frac{2}{3}.\left(W+2.C_2\right)A_1.\left[\left(V_d+V_{b1}\right)^{3/2} - V_{b1}^{3/2}\right] + A_1^2\left[\left(V_y+V_{b1}\right)^{2} - V_{b1}^{2}\right]\right]$$

$$I_d = \frac{C_1}{L}\left[C_2WV_d - \frac{2}{3}\left(W+2C_2\right)A_1\left[\left(V_d+V_{b1}\right)^{3/2} - V_{b1}^{3/2}\right] + A_1^2\left[V_d^{2} + V_{b1}^{2} + 2V_dV_{b1} - V_{b1}^{2}\right]\right]$$

$$I_d = \frac{C_1}{L}\left[C_2WV_d - \frac{2}{3}\left(W+2C_2\right)A_1\left[\left(V_d+V_{b1}\right)^{3/2} - V_{b1}^{3/2}\right] + A_1^2\left[V_d^{2} + 2V_dV_{b1}\right]\right] \qquad (10)$$

Therefore, the resistance of the pinch resistor will be

$$R = \frac{V}{I_d} \qquad (11)$$

IV. PINCH RESISTOR

Resistances at different voltages with different w

(a) At $N_d = 5*10^{16}$ cm^{-3} & $X_{J1} = 1um$

Table 1. For simple model

Voltage (V)	W=2.5μm R (10^4?)	W=5μm R (10^4?)
1	2.3951	1.1195
2	2.5174	1.1544
3	2.6268	1.1848
4	2.7288	1.2123
5	2.8261	1.2378

Table 2. For JFET model

Voltage (V)	W=2.5μm R (10^4?)	W=5μm R (10^4?)
1	2.2916	1.0912
2	2.3756	1.1147
3	2.4407	1.1331
4	2.4982	1.1493
5	2.5514	1.1641

(b) At N_d=5*10^{17} cm^{-3} & X_{j1}=1um

Table 3. For simple model

Voltage (V)		W=2.5 m R (10^4?)		W=5 m R (10^4?)
1		0.45822		0.22717
2		0.46092		0.22803
3		0.46320		0.22876
4		0.46521		0.22940
5		0.46703		0.22997

Table 4. For JFET model

Voltage (V)		W=2.5 m R (10^4?)		W=5 m R (10^4?)
1		0.45643		0.22661
2		0.45803		0.22711
3		0.45938		0.22754
4		0.46059		0.22793
5		0.46170		0.22828

(c) At N_d=5*10^{16} cm^{-3} & X_{j1}=3um

Table 5. For simple model

Voltage (V)		W=2.5 m R (10^5?)		W=5 m R (10^4?)
1		0.9345		4.3720
2		1.0262		4.7059
3		1.1123		5.0168
4		1.1970		5.3177
5		1.2820		5.6152

Table 6. For JFET model

Voltage (V)		W=2.5 m R (10^5?)		W=5 m R (10^4?)
1		0.8409		4.0814
2		0.9114		4.3118
3		0.9629		4.4908
4		1.0082		4.6500
5		1.0504		4.7996

(d) At N_d=5*10^{17} cm^{-3} & X_{j1}=1um

Table 7. For simple model

Voltage (V)		W=2.5 m R (10^3?)		W=5 m R (10^3?)
1		4.5822		2.2717
2		4.6092		2.2803
3		4.6320		2.2876
4		4.6521		2.2940
5		4.6703		2.2997

Table 8. For JFET model

Voltage (V)		W=2.5 m R (10^3?)		W=5 m R (10^3?)
1		4.5643		2.2661
2		4.5803		2.2711
3		4.5938		2.2754
4		4.6059		2.2793
5		4.6170		2.2828

(e) At N_d=5*10^{17} cm^{-3} & X_{j1}=3um

Table 9. For simple model

Voltage (V)		W=2.5 m R (10^4?)		W=5 m R (10^3?)
1		1.4462		7.1700
2		1.4603		7.2244
3		1.4721		7.2703
4		1.4826		7.3109
5		1.4922		7.3477

Table 10. For JFET model

Voltage (V)		W=2.5 m R (10^4?)		W=5 m R (10^3?)
1		1.4365		7.1338
2		1.4451		7.1661
3		1.4522		7.1933
4		1.4585		7.2177
5		1.4642		7.2399

Fig. Of Pinch resistor for simple model for:-
$N_{d=}$ 5*10^{16}/ cm^3, w=2.5um, xj1=1um.

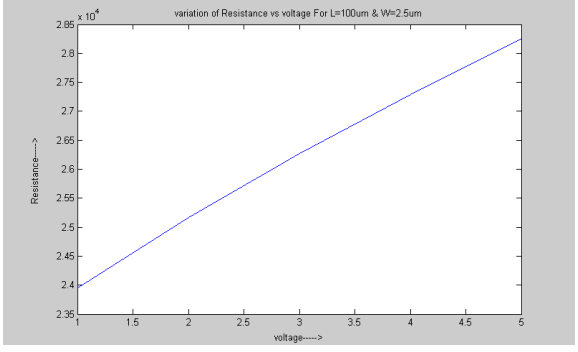


Fig. of the pinch resistor for simple model:-
N_d=5*10^{16}/cm^3, W=2.5um , X_{j1}=3um

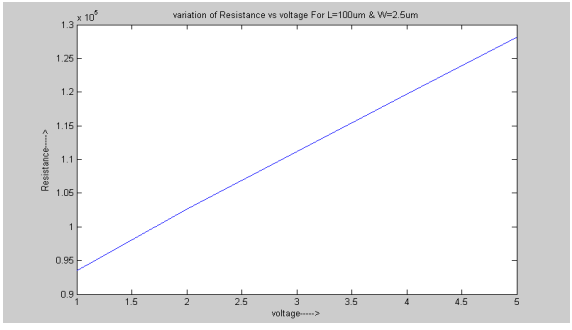


Fig. of the for pinch resistor for simple model :-
$N_d=5*10^{16}/cm^3$, W=5um , X_{j1}=3um

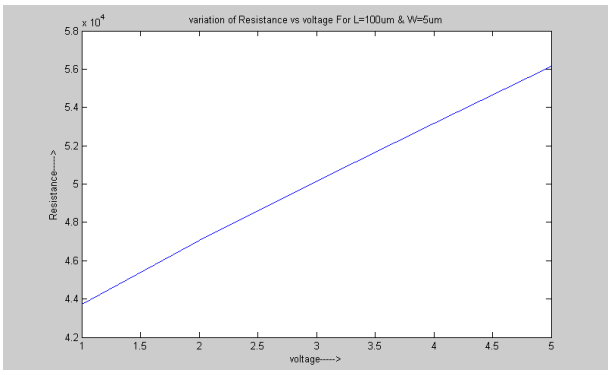


Fig.of Pinch resistor for simple model:-
$N_d= 5*10^{17}/cm^3$, W=2.5um, X_{j1}=1um

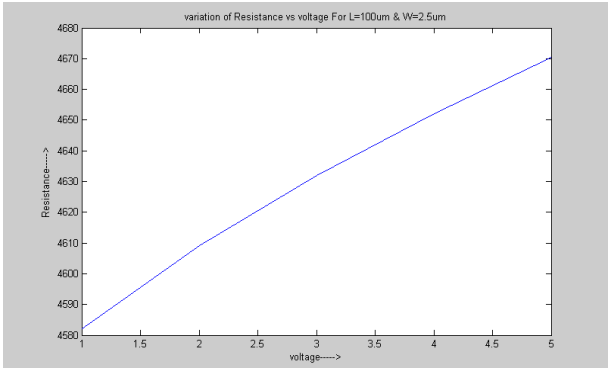
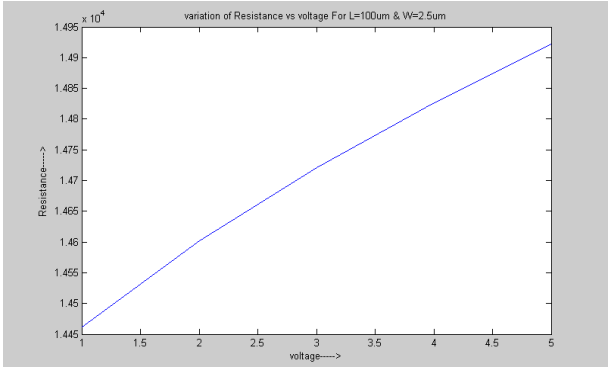


Fig .of pinch resistor for simple model:-
$N_d=5*10^{17}/cm^3$, W=2.5um , X_{j1}=3um



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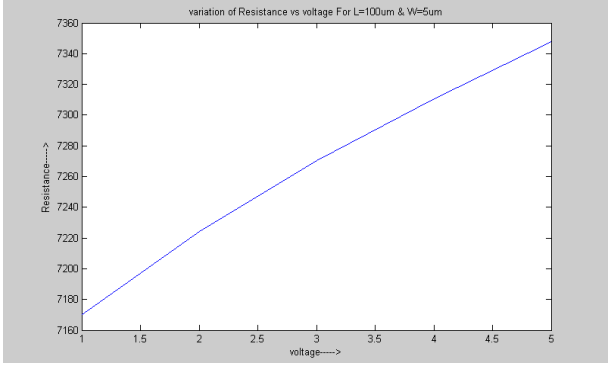


Fig of pinch resistor for JFET model for:-
$N_d=5*10^{16}/cm^3$,W=2.5um , X_{j1}=1um

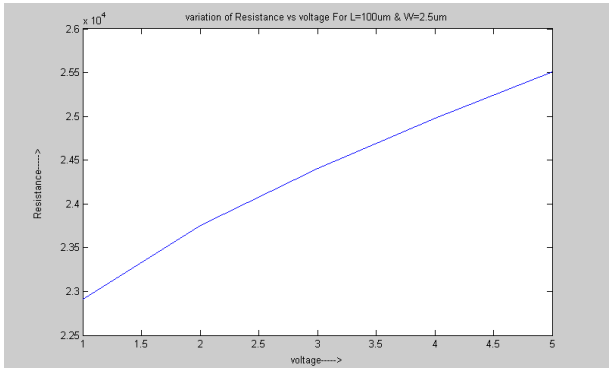


Fig .of Pinch resistor for JFET model for:-
$N_d=5*10^{16}/cm^3$, W=5um , X_{j1}=1um

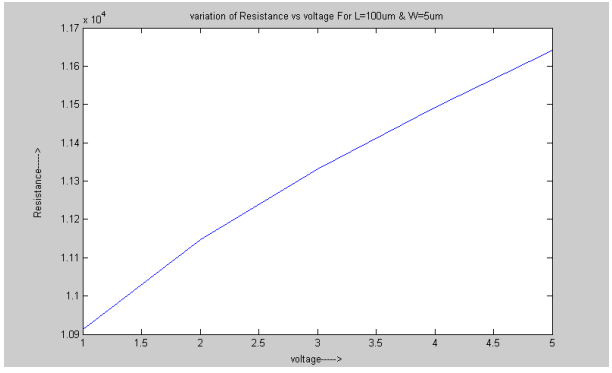


Fig. of the pinch resistor for the JFET model for :-
$N_d= 5*10^{16}$, W= 2.5um ,X_{j1}=3um

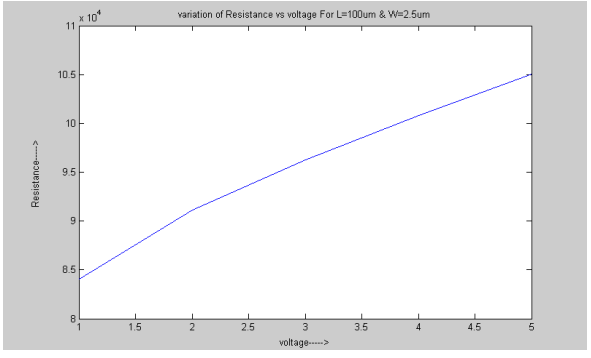


Fig.of Pinch resistor for the JFET model for:-
$N_d=5*10^{16}/cm^3$, W=5um ,X_{j1}=3um

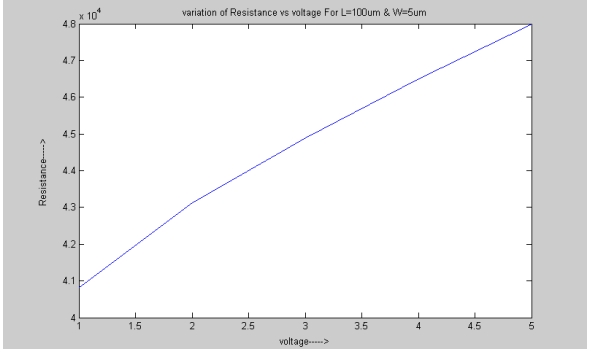


Fig. of pinch resistor for JFET model for:-
N_d=5*10^{17}/cm^3 , W=2.5um , X_{j1}=3

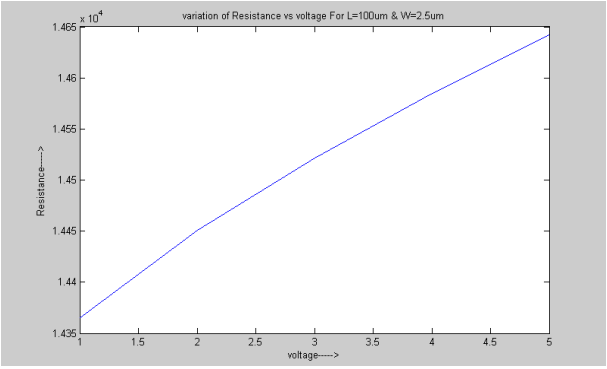
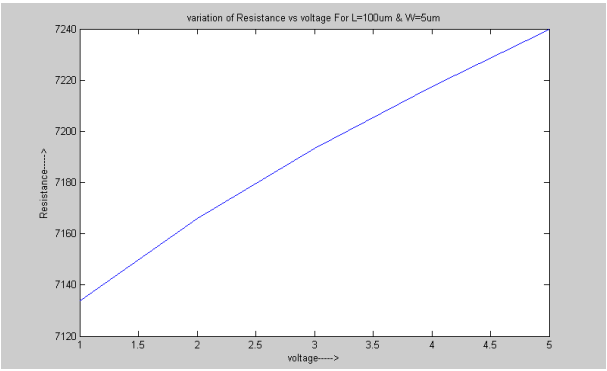


Fig.of Pinch resistor for JFET model for:-
N_d=5*10^{17}/cm^3 , W=5um ,X_{j1}=3



V. CONCLUSION

In this paper analytical modeling of pinch resistor has been carried out using the simple model and JFET model. The results obtained through the simple model are compared with the JFET model, which shows that the JFET model is more roburst for the VLSI design. For the same channel width and doping concentration for N_d= 5*10^{16}/cm^3, the resistance of the pinch resistor 1.44 times greater than the N-welll device resistor, and for the doping concentration N_d=5*10^{17}/cm^3,the resistance of the pinch resistor 1.35 times greater than the N-well device resistor.

For the same channel width and doping concentration for N_d= 5*10^{16}/cm^3,the resistance of the pinch resistor(for depth of the layer P^+ X_{j1}=3um) 6 times greater than the N-welll device resistor, and for the doping concentration N_d=5*10^{17}/cm^3,the resistance of the pinch resistor (for depth of the layer P^+ X_{j1}=3um) 4.2 times greater than the N-well device resistor.

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