DESIGN OF AREA-DELAY EFFICIENT ADDER BASED CIRCUITS IN QUANTUM DOT CELLULAR AUTOMATA

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Abstract—

Background: Semiconductor industry has achieved almost exponential scaling down in feature size and has no 100% solution in leakage current in CMOS. To replace CMOS technology, researchers done at nanoscale in recent years. Among emerging technologies, QCA plays an important role. QCA can implement digital circuits with high speed, small size and reduced power consumption. Our aim is on designing of different types of adder circuits in QCA. **Objective**: Our objective is to minimize the area, latency and also the number of cells in adder circuits in QCADesigner. **Results**: The proposed design reduces the number of cells and area compared with the available structures. By using QCA cells, different types of adders were designed Then they were simulated using QCADESIGNER tool. The performance can be analysed with the number of clock cycles. **Conclusion**: Experimental results show that the performances of proposed design of adders are more efficient than conventional designs.

I. INTRODUCTION

Now a days, Nanoelectronics seems to be the most emerging technology in both the field of engineering and electronics. Power consumption due to leakage current is significant in CMOS. VLSI technology, although has made remarkable progress in the past, this progress may be slowed down in future. However, it will be hard to sustain VLSI technology. As more and more devices are packed into the same area, the heat generated can no longer dissipate and may result in damage to the chip. QCA[1-2] provides a good alternative to the silicon technology. . A quantum dot is a particle of matter which is of small and it is dimensionless. All atoms are quantum dots. In nanotechnology, they are called quantum bits or qubit. Quantum Dot Cellular Automata (QCA) is considered as an emerging nanotechnology. Due to its merits, it is an alternative solution for CMOS technology. QCA is the zero dimensional nanostructure that can be used to design logical circuits A device based on QCA cells breaks away from FET based logic, and also exploits the quantum effects that come with small size and low power consumption [3]. Using QCA cells with dots of 20 nm diameter, an entire full adder can be placed within 1 μm^2.

The basic element of QCA is a quantum cell. A single quantum cell has electrons inside. QCA is an advanced research program and efforts are made to reduce the cells in the circuits. When the featured size is minimized to nanometer than Quantum effects such as Tunneling takes place [1]. QCA circuits can be directly obtained from conventional designs with addition of special clocking system. This results in efficient transmission of conventional circuits to get transformed into QCA structures. QCA uses polarization effect rather than conventional current for the transmission of information which contains the digital information. Thus a cell transfers the information throughout the circuit. The advantages of QCA include: Small size, High packing density, Consumes less power, High speed and Reduce the device error rates. Also QCA circuits have the advantage of high parallel processing.

The physical implementation of an automaton using quantum-dot cells automaton quickly gained popularity by replacing the CMOS technology[4-5].Method [6] describes the different XOR gate structures in quantum dot cellular automata. Method [7] describes a full adder layout with 150 cells and 9 Majority Gate with 2.25 delay and area of 0.28 μm^2. The full adder circuit with 292 cells and area of 0.62 μm^2 with 3.5 clock cycles and the full adder circuit with 220 cells with 3 closk cycles delay and area of 0.36 μm^2.This results in increase in number of clock cycles and cells [8-9].A 64-bit binary adder

exhibited a delay of only nine clock cycles, occupied an active area of 18.72 μm^2 [10].

II. QCA DESIGN SCHEME

A. QCA Cells

The fundamental QCA logic circuit cells have the Majority gate (MG) and Inverter [5] is shown in Fig.1(e) and (d). In each QCA cell has four quantum dots and inside the QCA cell has two free electrons. The electrons location will determine the binary states logic 1 and logic 0 [11]. Tunneling action only occurs within the cell and no tunneling happens between cells. The two charge configurations can be used to represent binary "0" and "1" with a polarization of –1 and +1 is shown in Fig.1(a) [5]. When a second cell is placed near the first cell, due to the coulomb interaction between the cells degeneracy were removed and then determines the ground state of the first cell[12]. Since no electrons tunnel between cells, QCA is used for transferring of information without current flow.

B. QCA wire crossings

One of the QCA's characteristics is the capability to create different signal wire crossings. In QCA technology, there are two crossover options: coplanar crossings and multilayer crossovers. A coplanar crossing implements crossovers by using only one layer is shown in Fig.1(b)[13]. The other alternative is a multilayer crossing in which it uses more than one layer of cells similar to the routing of metal wires in CMOS technology [14]. Multilayer crossovers are expected to achieve more reliable results in simulations. Multilayer crossovers are not easy to fabricate due to the multiple layer structure is shown in Fig.1(c), and the cost to fabricate a multilayer crossover is high than that of a coplanar crossing.

C. QCA clocks

Clock is a reference signal which controls timing in sequential CMOS circuits, whereas timing in QCA technology is performed by clocking in four periodic phases [15-16] such as switch, hold, release and relax is shown in Fig.2(a). The four-phase clocking scheme is called Landauer clocking and is used to modulate the inter-dot tunneling barrier of QCA cells. During the switch phase, in which actual computations are occurred, barriers are raised and a cell is affected by the polarization of its neighbors and a distinctive polarity is obtained. During the hold phase, barriers are high and the polarization of the cell is retained. During the release phase, barriers are lowered and the cell loses the polarity. In the relax phase, the cell is non-polarized [17].Clocking in QCA not only controls data flow but also serves as the power supply

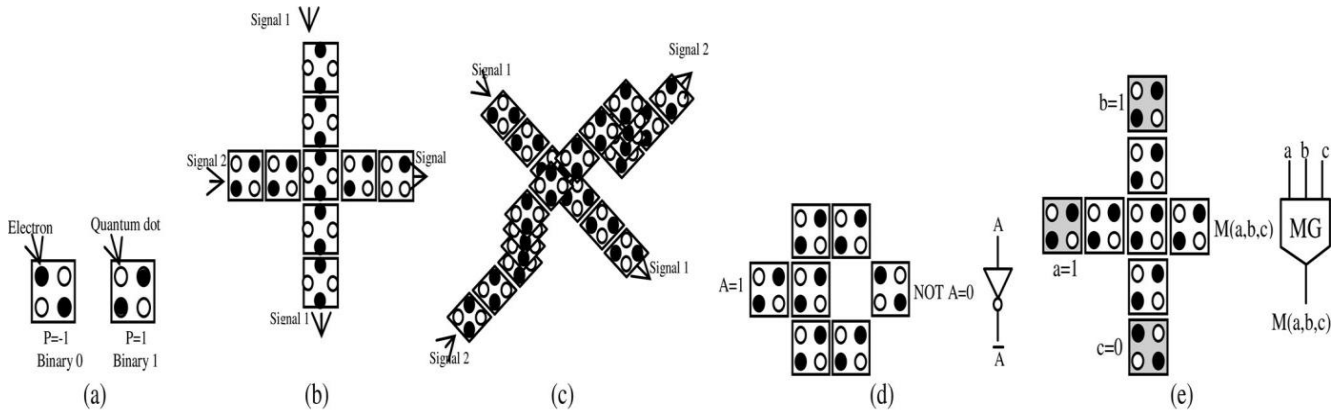


Fig.1. QCA elementary structures: (a) stable states of the basic cell; (b) coplanar crossing wires; (c) multilayer wires; (d) the inverter; (e) MG.

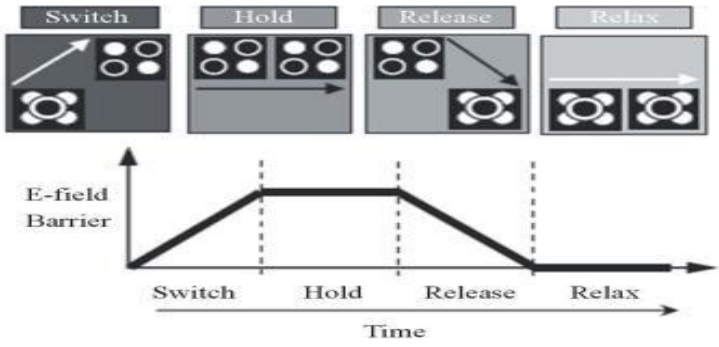
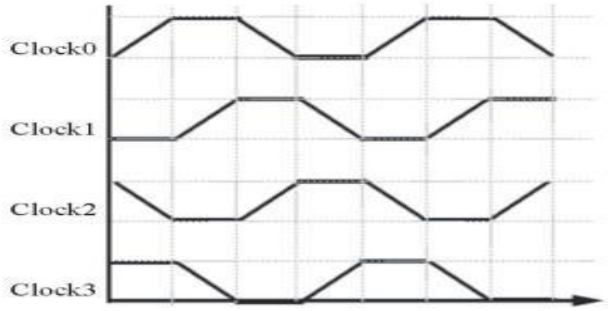


Fig.2. (a) Four phases of QCA clock;



(b) Clock zones signal.

III. QCADESIGNER TOOL

There are numerous designs and simulation tools for QCA circuits that has been developed by using approximations with low computational complexity, which can be used for relatively large scale circuit layout and simulation. These tools include MAQUINAS, QBART and QCADesigner [17]. Of these simulation tools, QCADesigner is the state-of-the-art and the most widely used QCA simulation tool. QCADesigner is the most popular simulation tool for semiconductor QCA circuit design. With the current version, QCADesigner ver 2.0.3,the circuit functionality is verified. There are two simulation engines: the bistable engine and the coherence vector engine.

In the current QCADesigner version 2.0.3, the size of the basic quantum cell was set at 18 nm by 18 nm with 5 nm diameter quantum dots. The center-to-center distance is set at 20 nm for adjacent cells. Research with silicon atom dangling bonds [18] shows the potential to operate at room temperature with cell sizes [19] on the order of 2 nm *2 nm, which minimizes the area by two orders of magnitude.

IV. PROPOSED METHOD

A. Half Adder

Half adder is a combinational circuit which performs addition of two operand bits. A half adder circuit is defined as follows in equations (1) and (2) is given in the literature.

$$Sum = M (M (A', B, 0), M (A, B', 0), 1) \quad (1)$$

$$Carry = M (A, B, 0) \quad (2)$$

Half adder can be designed by using QCA gates with three majority gate and an inverter. The inputs are A and B and is given to two majority gates M1 and M2 which acts as an AND gate. The output of the AND gate is given to another majority gate M3.The output of majority gate 3 is the sum and that of majority gate 4 is the carry. The logic diagram and the layout in QCADesigner is shown in figure 3 and 4. It is seen that the half adder circuit is nothing but a XOR gate which is realized using QCA basic gates.

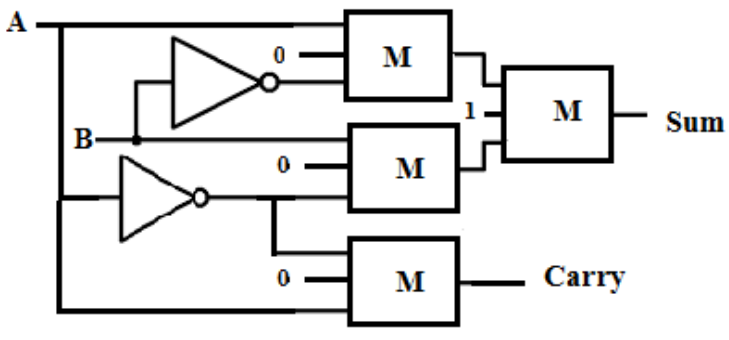


Fig.3. Logic Diagram of Half adder using QCA

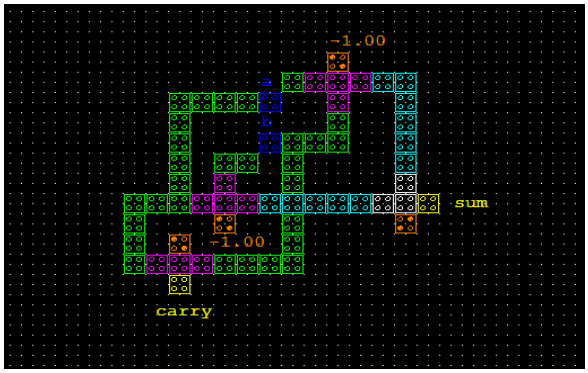


Fig.4. Layout of Half adder using QCA gates.

B. Full Adder

Full adder circuit can be implemented using digital logic gates. To implement the complete circuit of a one bit full adder, used 3 Majority gate and 2 inverters. A full adder circuit is defined as follows in equations (3) and (4).

$$\text{Sum} = M (M' (A, B, C), M (C', A, B), C) \quad (3)$$

$$\text{Carry} = M(A,B,C) \quad (4)$$

Majority gate M1 has three inputs and are A,B,C. The output of majority gate M1 is the carry. Majority gate M2 is a three input majority gate. A,B,C' acts as the inputs to majority gate M2 and the output is fed to the majority gate M3. Majority gate M3 is also a three input gate whose inputs are C, output inverted from carry and output from majority gate M2.The logic diagram and layout is shown in Fig. 5 and6.

C. Multiplexer

In digital circuit design, the selector wires are of digital value. A 2:1 multiplexer is defined in equation (5) where A and B are the two inputs, S is the selector input, and Z is the output:

$$Z = M (M (A, S', 0) , M (B, S, 0), 1 \quad (5)$$

In order to realize multiplexer using QCA, we need three majority gate and an inverter. The circuit diagram and layout is shown in Fig. 7 and 8

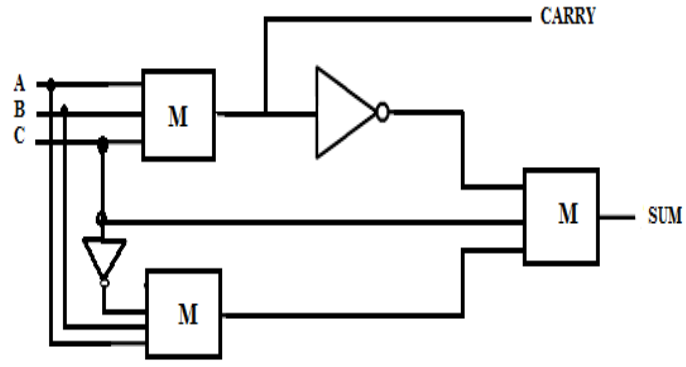


Fig.5. Logic Diagram of Full adder using QCA.

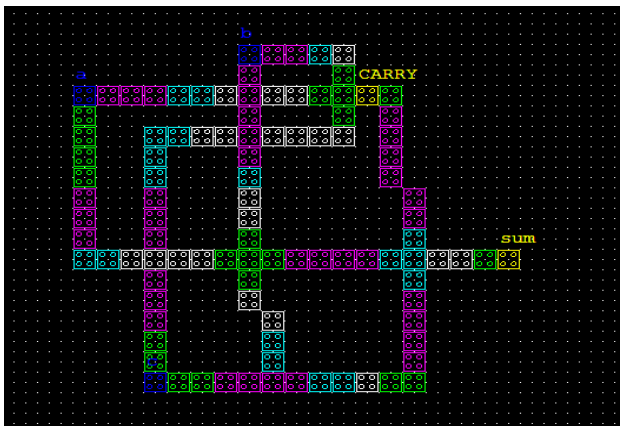


Fig.6. Layout of Full adder using QCA gates.

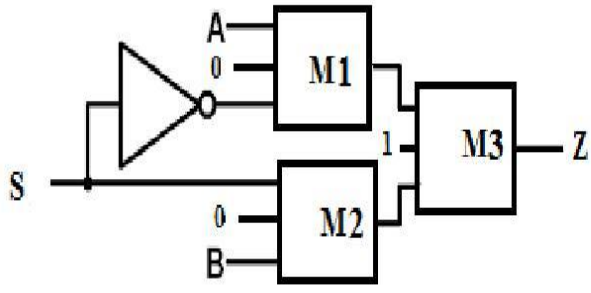


Fig.7. Circuit Diagram of Multiplexer using QCA.

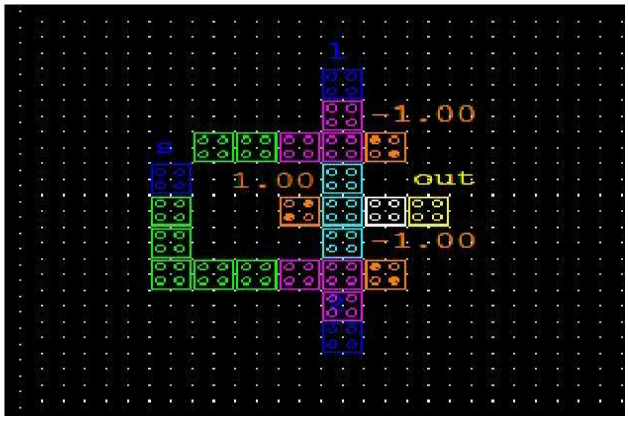
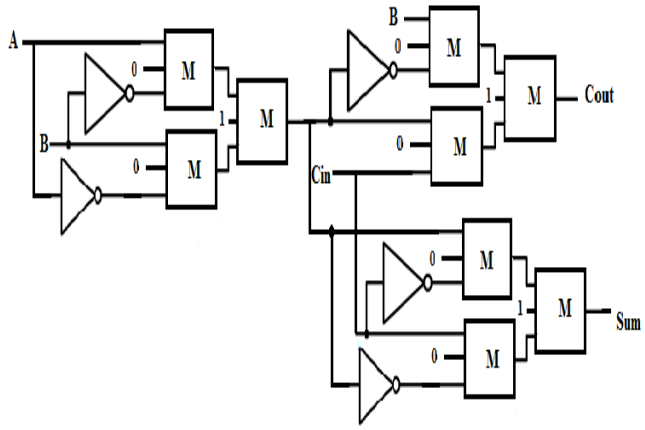


Fig.8. Layout of Multiplexer using QCA gates.



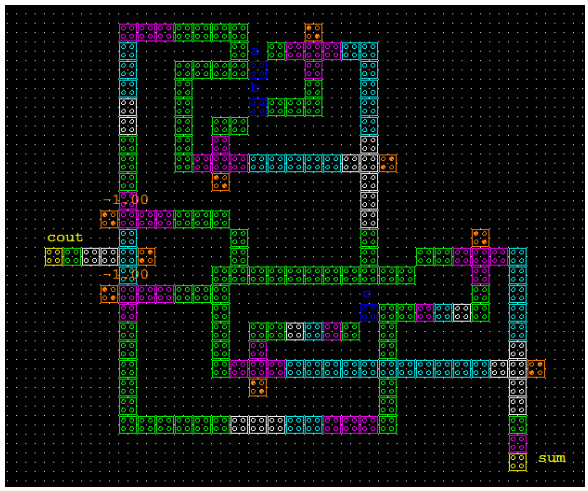
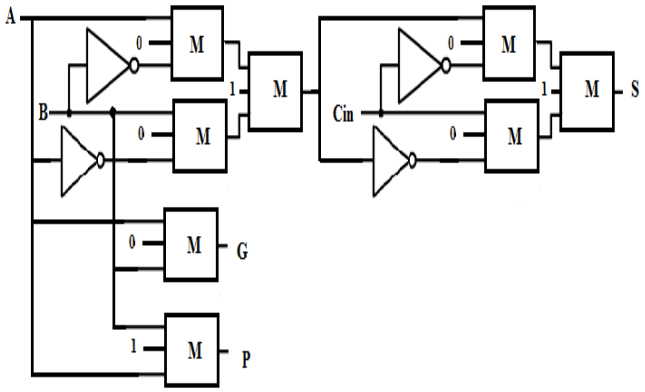


Fig.9.Logic Diagram of Full adder using Multiplexer using QCA. Fig.10. Layout of Full adder using Multiplexer using QCA gates.



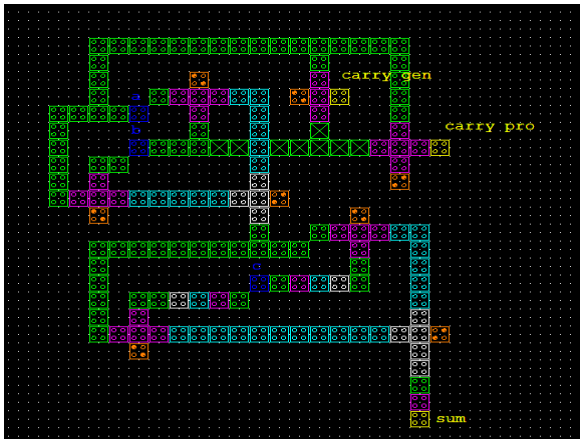


Fig.11. Circuit Diagram of 1 bit adder using QCA.

Fig.12. Layout of 1 Bit adder using QCA gates.

D. Bit adder block

The 1-bit adder block used in the carry-look ahead adder is shown in Fig.5. It has two XOR gates to produce the *S* sum output bit of the *A,B,Cin*(carry in) input bits. Therefore, a simple AND gate is sufficient to compute the generate-carry signal on the *G* output.The propagate carry signal on the *P* output is computed the OR gate by using majority gates and inverter is shown in Fig.11. The symbol in cross indicates the two wires are crossed over.

E. Carry Look Ahead adder

The layout of 2 bit Carry look ahead adder is shown in Fig.13.

V. RESULT ANALYSIS

If we compare the results with the available results, it will be seen that our proposed QCA structures reduces the delay, area and cell count. Complexity in terms of cell counts, delay and area consumption of QCA circuits can be easily obtained by QCADesigner and hence, the performance of the circuit will increase.

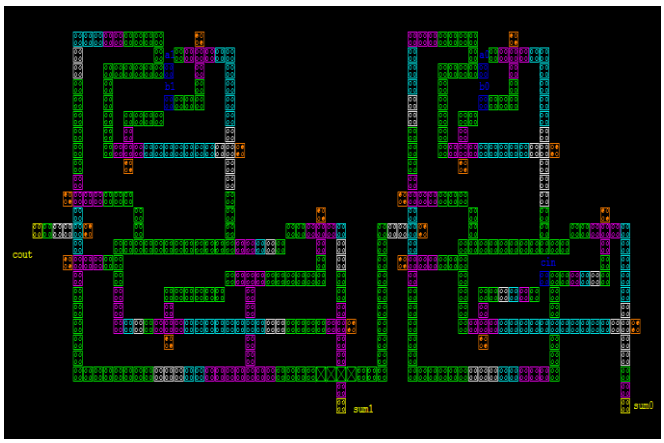


Fig.13. Layout of 2 Bit Carry look ahead adder using QCA gates.

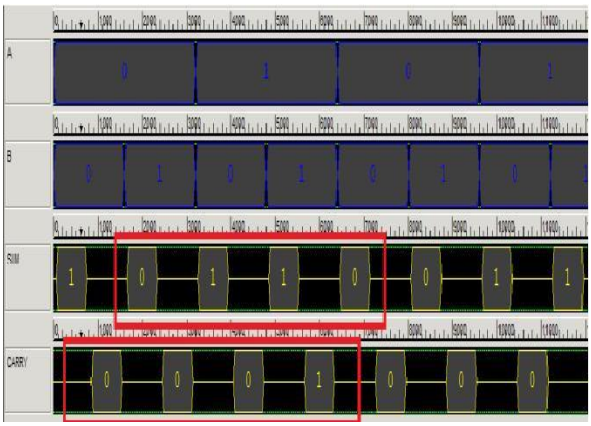


Fig.14. Simulation result of Half Adder.

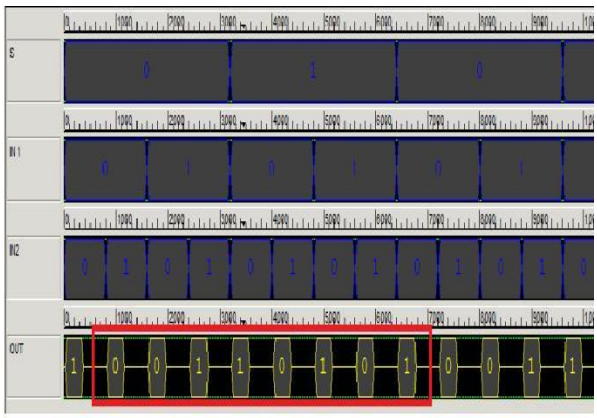


Fig.17. Simulation result of Multiplexer.

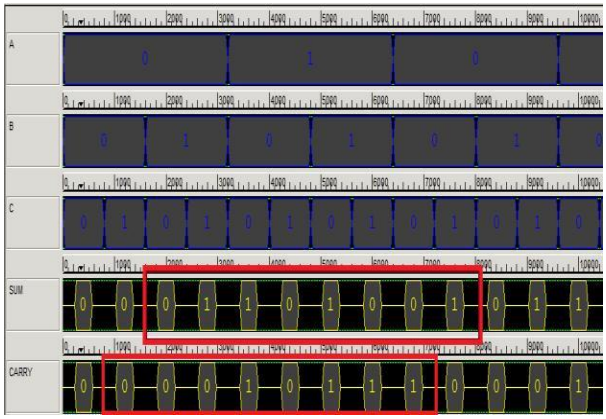


Fig.15. Simulation result of Full Adder

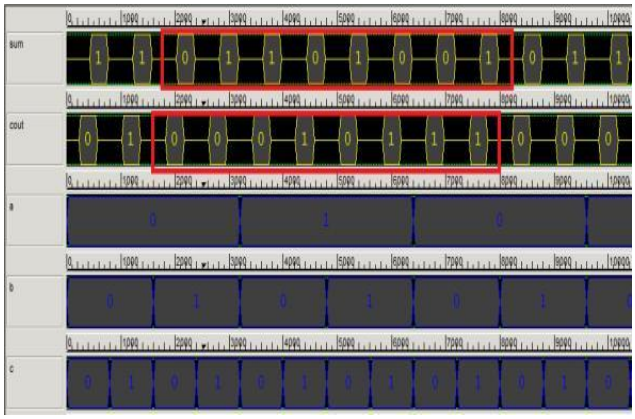


Fig.18. Simulation result of Full Adder using Multiplexer.

Fig.16.Simulation result of 1 Bit Adder

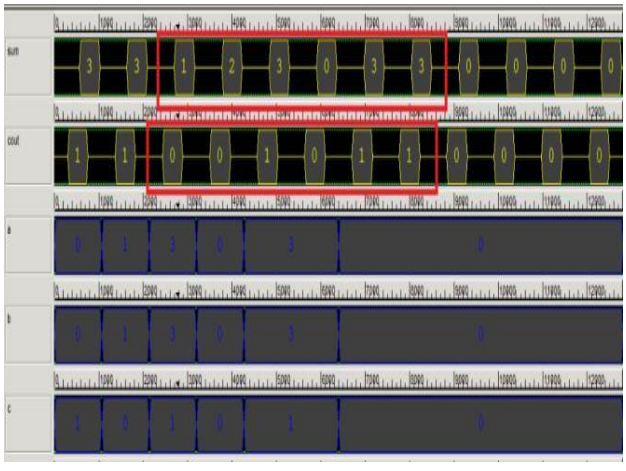


Fig.19.Simulation result of 2 bit Carry look ahead adder.

Table II demonstrates the comparison between the QCA based adder circuits implementation and the results available in literature. The simulation result of the adder circuits obtained by the layouts in QCADesigner is given in Fig.14-19.

TABLE I. Comparative study of adder circuits with the results available in literature.

QCAstructures	Previous structures				Proposed structures			
	Paper	Cell count	Area (μm²)	Latency	Figures	Cell count	Area (μm²)	Latency
Half adder	[7]	63	0.11	1				
	[20]	77	0.08	1	Fig.4	62	0.09	1
Full adder	[7]	150	0.28	2.25				
	[8]	292	0.62	3.5	Fig.6	101	0.15	2
	[9]	220	0.36	3				
Multiplexer	[21]	49	0.06	2	Fig.8	24	0.04	1
Full adder using Multiplexer	NA	NA	NA	NA	Fig.10	179	0.27	2
1 Bit adder block	[8]	292	0.62	3.5	Fig.12	155	0.22	2
Carry look ahead adder	CLA4 [22]	1758	3.2	4	CLA2 Fig.13	404	0.62	2

VI. CONCLUSION

From this paper the design, layout and simulation of adder circuits has been studied. The proposed designs shows the implementations of QCA based circuits using reduced number of QCA cells so that the power consumption in such circuits will obviously be low. The adder structures, are an efficient building block for larger arithmetic structures. The simulation results of half and full adder circuits have been verified using QCADesigner. These structures have been found to have less delay and better throughput compared to other structures. The circuit area was also found to be reduced. Simple QCA structures can be designed with basic gates. In addition, results are verified by the truth table.

VII. FUTURE SCOPE

As we discussed with only Adders, these are the fundamental requirements of logic gates. If the logic gates are designed, we can able to design different kind of circuits. The 2 bit adder circuits were designed and obtained the simulation results.. The QCA layouts and the simulation results are not only demonstrated but also will be analyzed for a clear understanding of the future work. QCA adder circuits will be useful as an efficient building block for larger arithmetic logic units (ALU) in future. Thus, the larger adder circuits will be designed with the minimum number of QCA cells and the simulation results will be obtained in future.

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